Department of Electronics and Instrumentation Engineering

M.Sc. (I & T) IV semester (2013-2014)

ELECTRICAL CIRCUITS DEVICES & DIGITAL LAB

LIST OF EXPERIMENTS

1. Characteristics of Semiconductor diode
2. Characteristics of Zener diode
3. Characteristics of Bipolar Junction Transistor (BJT).
4. Fixed IC voltage Regulator.
5. Analysis of DC Resistive Circuits. (KVL, KCL) .
6. Simulation of Super position and Tellegen's theorem using Electronic Work Bench (EWB) Software.
7. Simulation of simple electronic circuits (OP-AMP based) using Electronic Work Bench (EWB) Software.
8. Implementation of Digital to Analog Converter using Millman's theorem.
9. Digital Multiplexer and De-multiplexer.
10. Verification of Logic Gates using Integrated Chips.
11. Implementation of Half adder and Half Subtractor using Logic gates.
12. Simplification of Boolean expression using Karnaugh map.

CIRCUIT DIAGRAM :

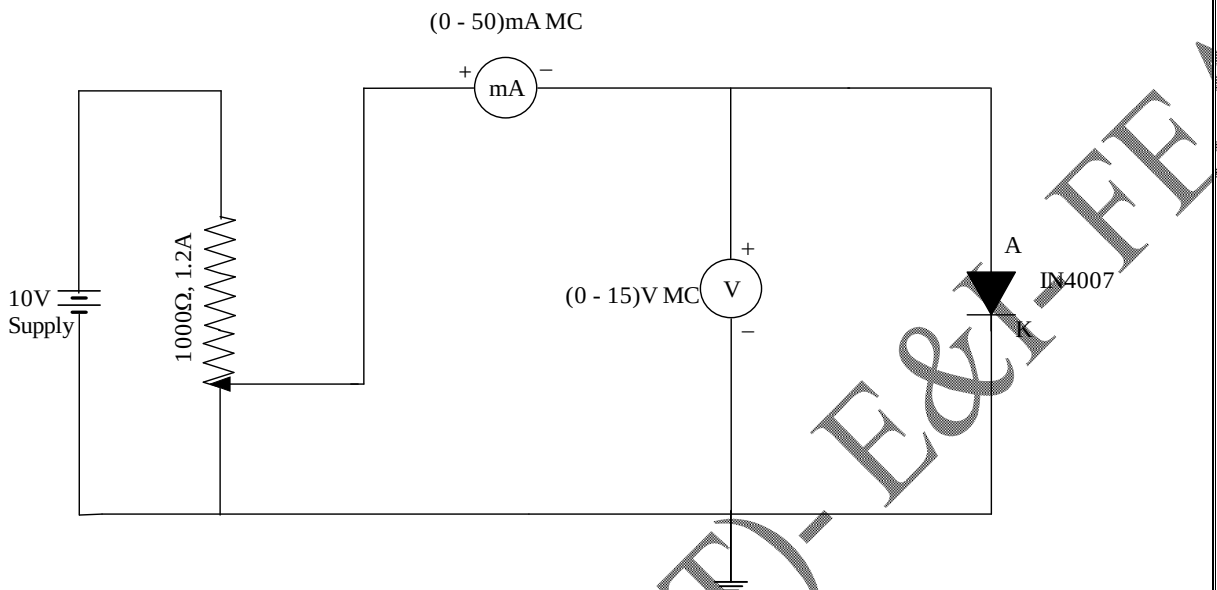


Figure.1 Forward Bias

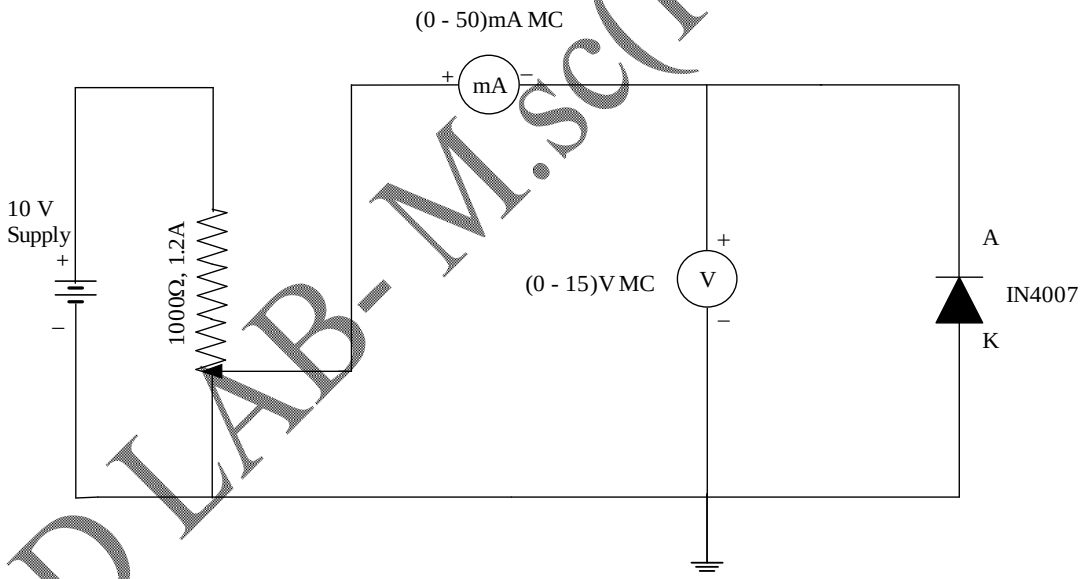


Figure.2 Reverse Bias

EXP NO:
DATE:

CHARACTERISTICS OF SEMI-CONDUCTOR DIODE

AIM:

To obtain the volt-ampere characteristics of the semi-conductor diode.

EQUIPMENTS REQUIRED:

DC voltage source	– 1 No.
Potential divider (1000Ω, 1.2A)	– 1 No.
Milli ammeter (0 - 50mA)	– 1 No.
Voltmeter (0 - 30V)	– 1 No.
Diode (IN 4007)	– 1 No.

THEORY :

Diode is a 2 layer uni-directional semi-conductor device. It has 2 terminals. i.e anode(A) and cathode (K). It will conduct only in the forward bias and not in reverse bias. This means that it provides very low resistance in the forward bias and a very high resistance in the reverse bias. It is used in the rectifier circuit for converting AC to DC.

PROCEDURE:

(a) Forward Bias:

(i) Connections are given as per the circuit diagram shown in Figure.1.
(ii) By varying the potential divider from zero to maximum, corresponding voltmeter and ammeter readings are noted.
(iii) The above readings are tabulated and a graph is drawn with anode cathode voltage (V_{AK}) along X-axis and current (I_{AK}) along Y-axis.
(iv) Find D.C forward resistance and A.C forward resistance as explained in the model graph.

(b) Reverse Bias:

(i) Connections are given as per the circuit diagram shown in Figure.2.
(ii) By varying the potential divider from zero to maximum, corresponding voltmeter and ammeter readings are noted.

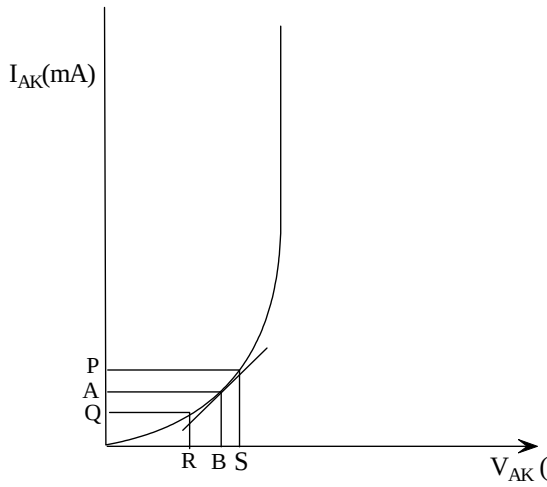
PRECAUTION:

(i) The potential divider should be kept at minimum potential position at the time of starting the experiment.
(ii) The junction diode should be connected with proper polarity.
(iii) Do not give connections when supply is switched ON.
(iv) Power supply should be switched ON only when the connections in the circuit are satisfied.

TABULATION:

Forward Bias		Reverse Bias	
V_{Ak} (volts)	I_A (mA)	V_{Ak} (volts)	I_A (mA)

MODEL GRAPH:



$$AC\ \ Forward\ \ \text{Re}\,sis\,\text{tan}\,ce = \frac{OS - OR}{OP - OQ}$$

$$DC\ \ Forward\ \ \text{Re}\,sis\,\text{tan}\,ce = \frac{OB}{OA}$$

RESULT:

The Volt-ampere characteristics of the semi-conductor diode were drawn.
The DC and AC Forward resistance were determined.

DC Forward resistance of the junction diode =
AC Forward resistance of the junction diode =

CIRCUIT DIAGRAM:

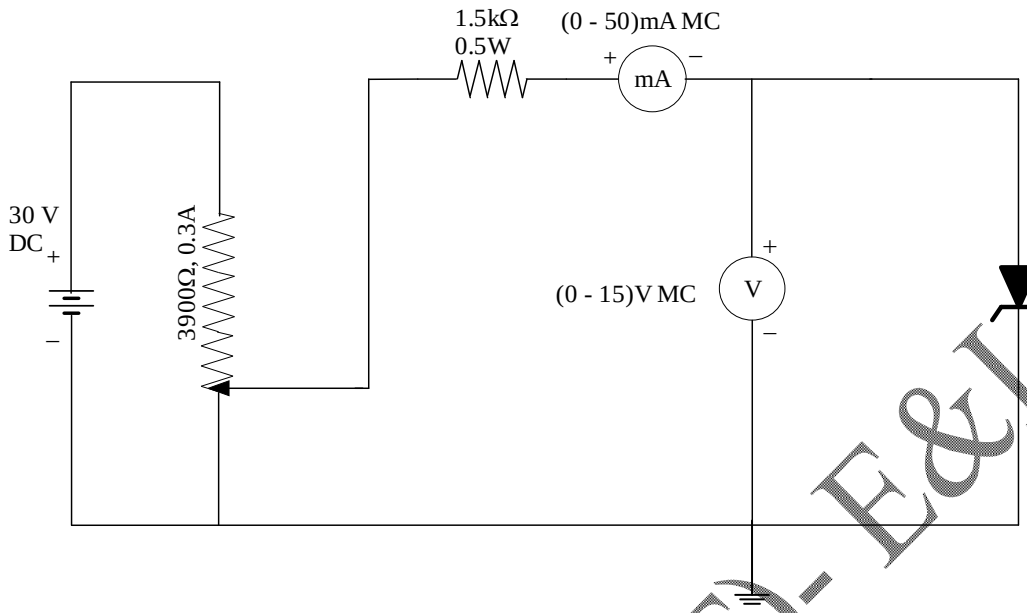


Figure. 1. Zener Diode in Forward Bias

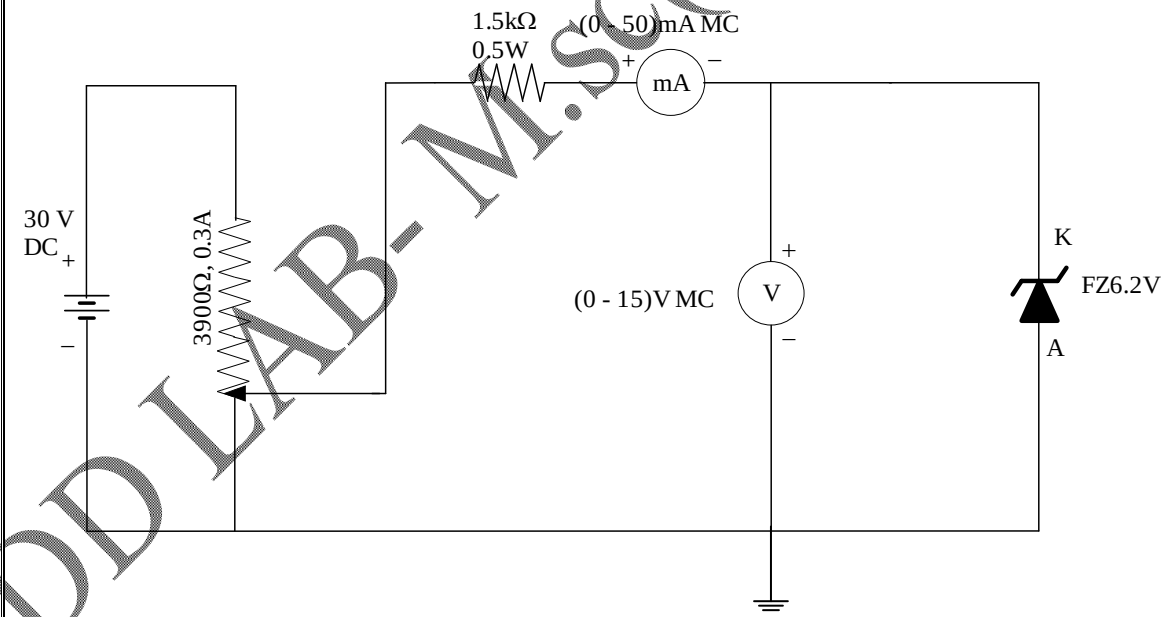


Figure. 2. Zener Diode in Reverse Bias

EXP NO:
DATE:

CHARACTERISTICS OF ZENER DIODE

AIM:

To obtain the Volt-ampere characteristics of Zener diode.

SPECIFICATIONS:

Nominal Zener voltage at I_Z	-	6.2 Volts
Test current I_Z	-	20 mA
Max. Dynamic impedance at I_Z	-	12 ohms
Max. Leakage current at V_{ZR}	-	10 µA
Leakage current test voltage V_{ZR}	-	3 Volts
Typical temp. Coefficient	-	$\pm$ 0.03

COMPONENTS REQUIRED:

(i) 30 Volts DC power supply.
(ii) 3900 ohms, 0.3 amp potential divider.
(iii) 0 – 50 mA, mc ammeter.
(iv) 0 -3 volts, mc voltmeter.
(v) 0 – 10 volts, mc voltmeter
(vi) Zener diode FZ 6.2V.
(vii) 1.5 kohm, 1/2 watt resistor.

THEORY:

Zener diode is a two layer bilateral semiconductor device. It is also called as a voltage-reference, voltage regulator or breakdown diode. It consists of a PN junction and it is mainly operated in the reverse breakdown region. The break down voltage of a zener diode is set by carefully controlling the doping level during manufacture. It is having two terminals named anode(A) and cathode (K).

APPLICATIONS:

Zener diode has a number of applications, yet the following applications are important.

(i) As a voltage regulator.
(ii) As a fixed reference voltage in transistor biasing circuits.
(iii) As peak clippers or limiters in wave shaping circuits.
(iv) For meter protection against damage.

TABULAR COLUMN:

FORWARD BIAS		REVERSE BIAS	
Forward Zener voltageV_{ZF} in volts	Forward Zener current I_{ZF} in mA	Reverse Zener voltage V_{ZR} in Volts	Reverse Zener current I_{ZR} in mA

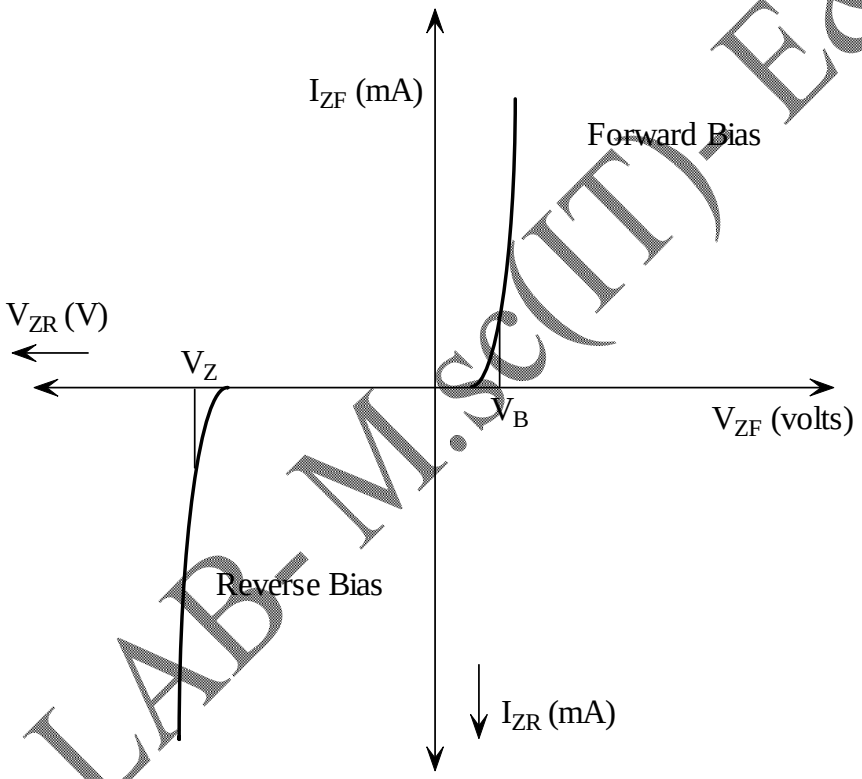
PROCEDURE:

(i) Give connections as per the circuit diagram.
(ii) Vary the potential divider in steps and note down the corresponding voltmeter and ammeter readings.
(iii) Same procedure is repeated by reverse biasing the zener diode.
(iv) Tabulate the readings and obtain the volt-ampere characteristics with voltmeter readings along X-axis and ammeter readings along Y-axis.

PRECAUTIONS:

(i) The potential divider should be kept at minimum potential position.
(ii) Zener diode should be connected with proper polarity.

MODEL GRAPH:



V_Z – Zener breakdown voltage
V_B – Zener break over voltage
V_{ZF} – Zener forward voltage
V_{ZR} – Zener reverse voltage
I_{ZF} - Zener forward current
I_{ZR} – Zener reverse current

RESULT:

The volt-ampere characteristic of zener diode was thus obtained.

EXP NO:
DATE:

CHARACTERISTICS OF A TRANSISTOR

AIM:

To determine the (i) Input characteristics and (ii) Output characteristics of the given transistor in common emitter configuration.

APPARATUS REQUIRED:

D.C Voltmeter (0-10V), (0-1V)
D.C Ammeter (0-100mA)&(0-100μA)
Rheostat of 3600 ohms and 0.3A
Transistor SL 100 (NPN Transistor)

THEORY:

Input characteristics:

Figure.1 shows a transistor in common emitter configuration. From Figure.1 it is clear that I_B & V_{BE} are the input quantities and I_C & V_{CE} are the output quantities. Study of input quantities keeping V_{CE} as constant gives input characteristics.

Output characteristics:

Study of output quantities keeping I_B as constant gives output characteristics.

PROCEDURE:

Input characteristics:

1. Give the connection as shown in Figure.1
2. Voltage between collector and emitter is fixed say at 1V by varying Rheostat V_{BE} is changed and corresponding I_B is noted
3. Collector to emitter voltage V_{CE} is fixed at say 2V, 3V etc and the above procedure is repeated
4. A graph between V_{BE} & I_B is drawn for various values of V_{CE}.

Output Characteristics:

1. Give the connection as shown in Figure.2
2. The base current is kept at a value say 25μA with the help of the rheostat. The variation of collector current is noted by varying the collector voltage.
3. Repeat the above procedure for I_B = 50μA & I = 75μA.
4. A graph between V_{CE} & I_C is drawn for various values of I_B.

CIRCUIT DIAGRAM:

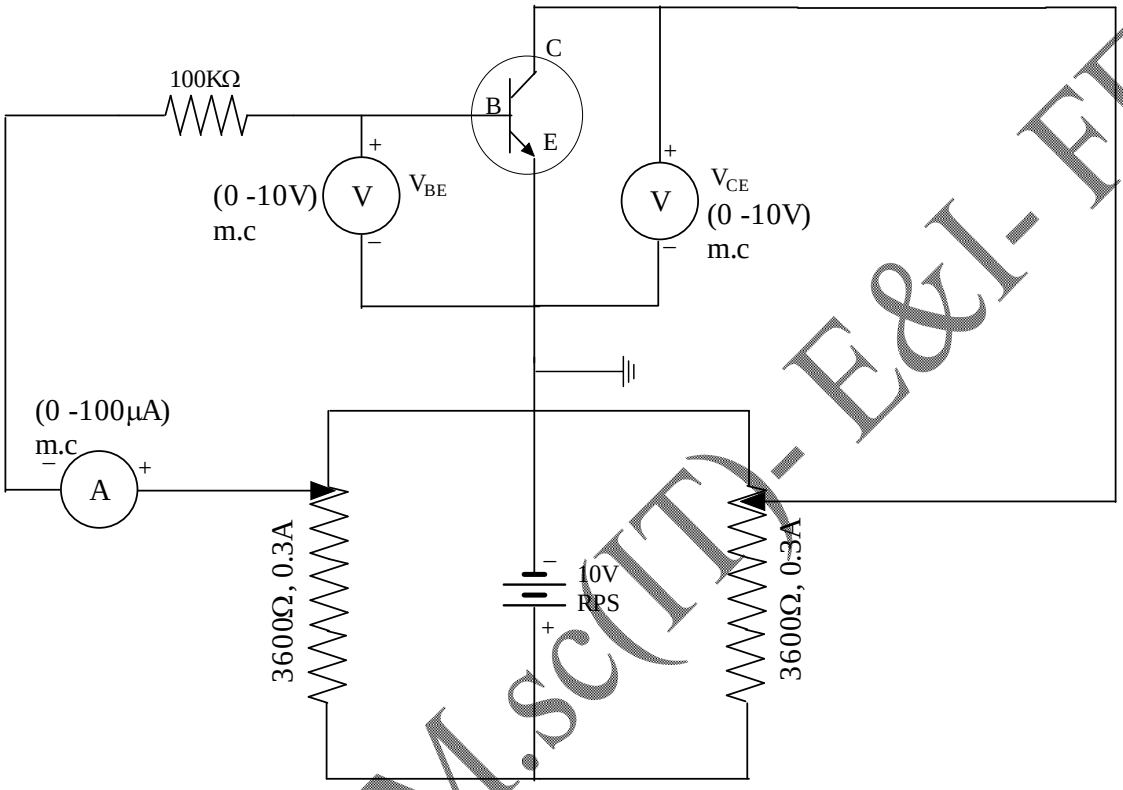


Figure.1 Input Characteristics

Table.1 Input Characteristics:

V_{CE} = Volts		V_{CE} = Volts		V_{CE} = Volts	
V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)

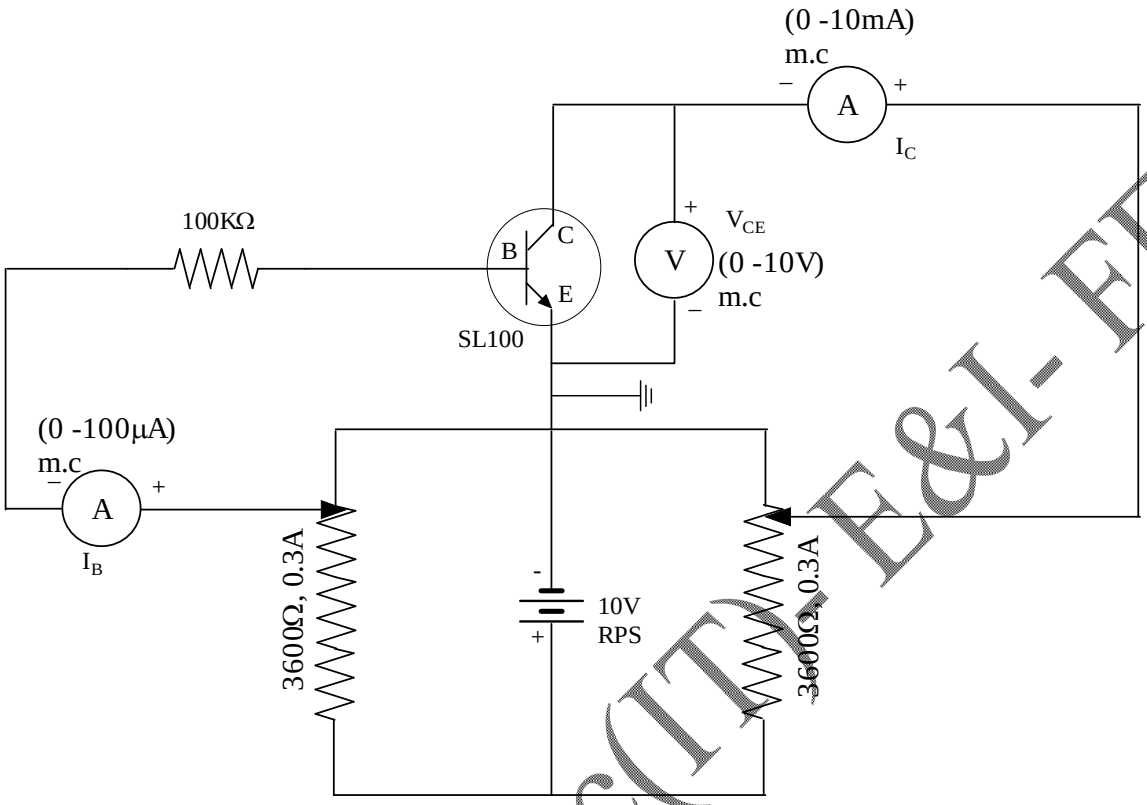


Figure.2 Output Characteristics

Table.2 Output Characteristics:

I_B = μA		I_B = μA		I_B = μA	
V_{CE} (V)	I_C (mA.)	V_{CE} (V)	I_C (mA.)	V_{CE} (V)	I_C (mA.)

MODEL GRAPH:

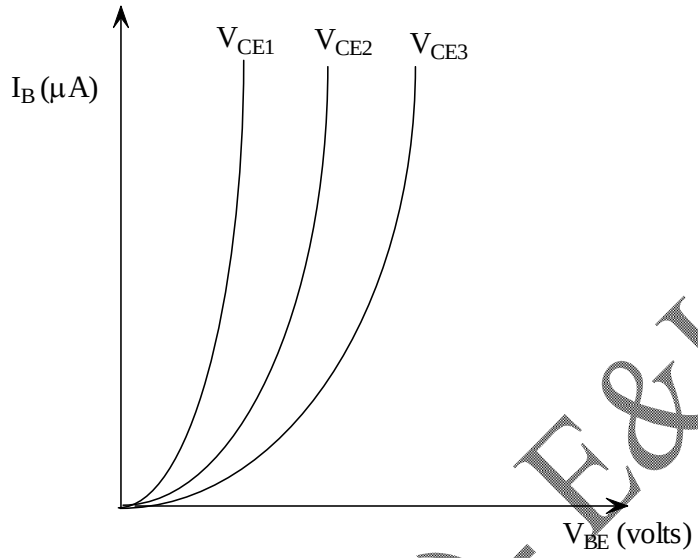


Figure.3 Input Characteristics

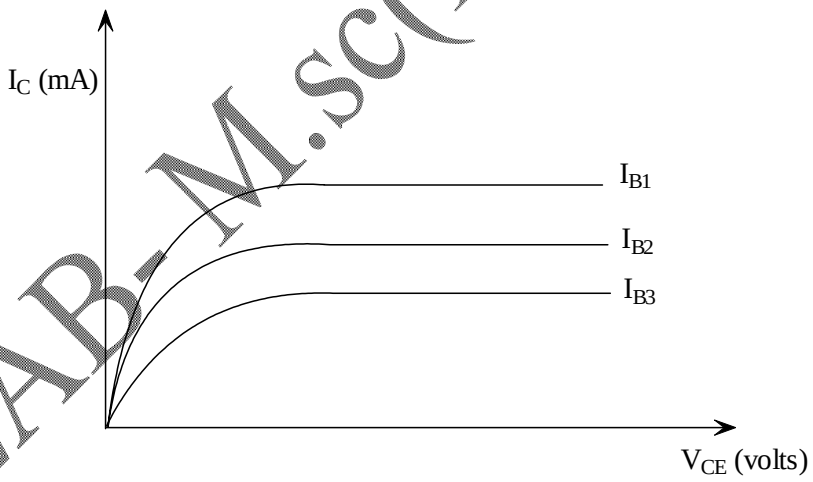


Figure.4 Output Characteristics

RESULT:

The experiment was conducted and the input & output characteristics were obtained.

EXP N0:
DATE:

FIXED IC VOLTAGE REGULATOR

AIM:

To construct a Fixed IC voltage regulator for Fixed voltage

COMPONENTS REQUIRED:

Auto Transformer 1φ, 230V/270V	– 1 No.
Step down Transformer 1φ, 230V/15V`	– 1 No.
Diodes (BY 127)	– 4 Nos.
IC – 7805	– 1No.
Capacitor 1000µF, 0.1µF	– 1No.
Milli ammeter (0 - 100mA)	– 1 No.
Voltmeter (0 - 40V)	– 1 No.
Rheostat 3.6KΩ, 0.3A	– 1 No.

SPECIFICATIONS OF IC 7805:

Output Voltage – 5V DC
Max. Input Voltage – 35V DC
Max. Output Current – 1A
IC 7805 is available in TO -220 plastic package

THEORY:

The 7800 series consist of three terminal positive voltage regulators with seven voltage options.

TYPE	OUTPUT VOLTAGE	MAX INPUT VOLTAGE
7805	5.0	35V
7806	6.0	35V
7808	8.0	35V
7812	12.0	35V
7815	15.0	35V
7818	18.0	35V
7824	24.0	40V

IC 7805 provides a constant output voltage of 5 volts for line and load variations. The proper operation requires a common ground between input and output voltage. In addition the difference between input and output voltages (Vin ~Vo) called DROPOUT voltage must be typically 2V. The capacitor C_i filters out the effect of stray inductance in the input wires and is required if the regulators are located at appreciable distance from a power supply. Filter capacitor C_o may be used to improve the transient response of the regulator to sudden load current changes.

PROCEDURE:

LINE VARIATION:

1. Give the connections as per the circuit diagram shown in Figure 2.
2. Now keep the unregulated input at 25V by increasing the auto transformer output voltage.
3. For taking the no load reading keep the SPST switch open and note down the output voltage.
4. Now decrease the input voltage in steps of 5V and note down the corresponding input and output voltages.

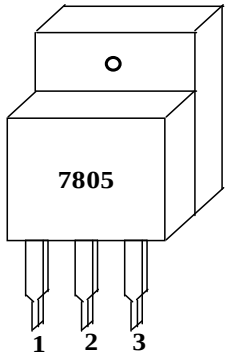
LOAD VARIATION:

1. Set the input voltage at pin 1 of 7805 at 25V and close the SPST switch.
2. Measure the output voltage for different load currents.

PRECAUTIONS

1. The output voltage of the auto-transformer should not exceed 230V.
2. The input voltage applied to IC7805 should not exceed 35V.

TO - 220 PLASTIC PACKAGE OF IC 7805



TYPICAL CIRCUIT CONNECTION FOR IC 7805

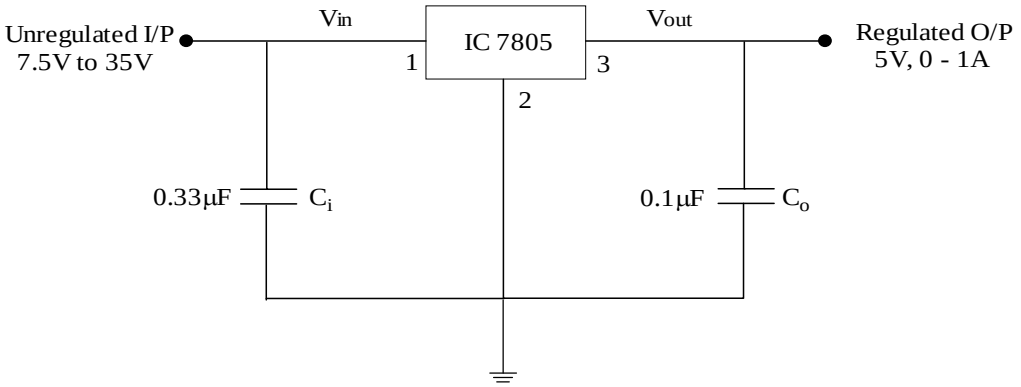


FIGURE 1

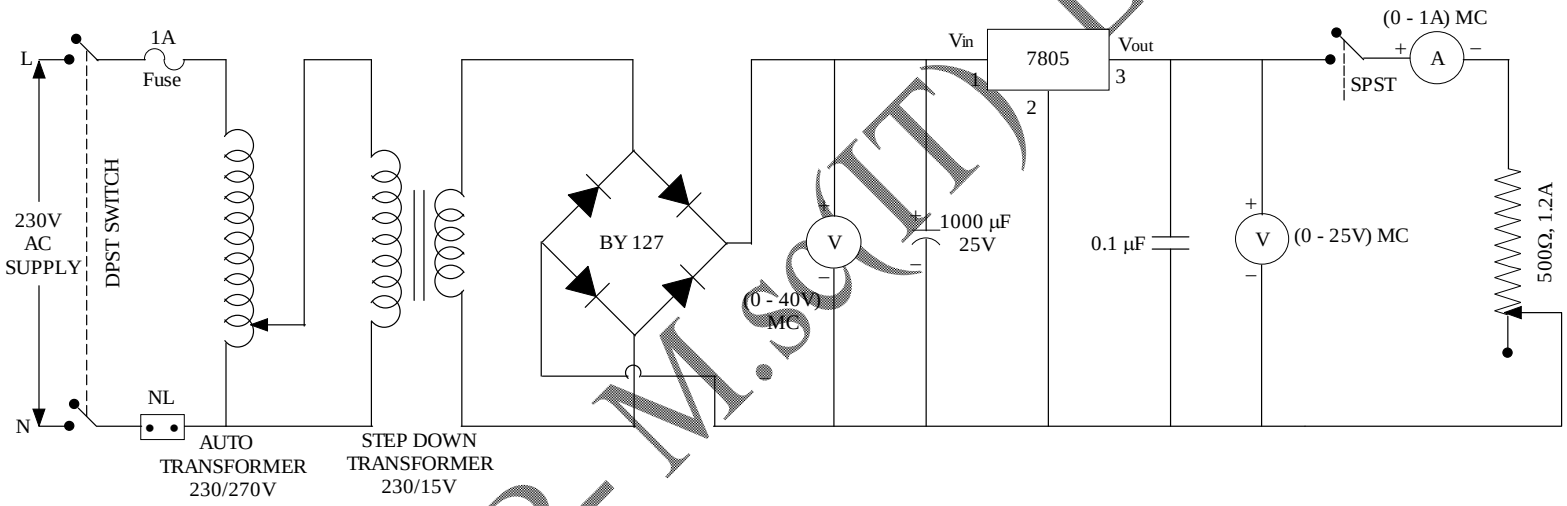


Figure. 1. Circuit Diagram

FIXED VOLTAGE REGULATOR:

Table. 1: Load Variation

$\mathbf{V_{out}}$ = **V**

Load Current (mA)	Output Voltage (Volts)

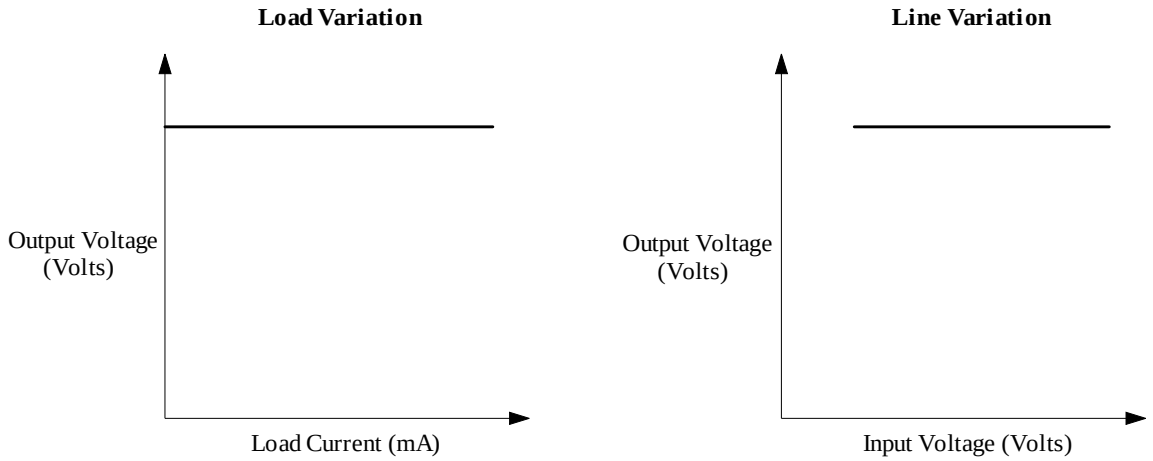
Table. 2: Line Variation

$\mathbf{V_{in}}$ = **V**

Input Voltage (Volts)	Output Voltage (Volts)

MODEL GRAPH:

FIXED VOLTAGE REGULATOR:



RESULT:

Thus Fixed IC Voltage Regulator was constructed and tested.

EXP NO:
DATE:

ANALYSIS OF DC RESISTIVE CIRCUITS

AIM :

To analyze the given DC circuit and verify Kirchoff's current law, Kirchoff's voltage law and Ohm's law experimentally.

COMPONENTS REQUIRED:

Resistor 100Ω, 200Ω	- 2Nos.
Resitor 470Ω	- 1No.
Dc power supply	- 2Nos.
Ammeter (0 -50 mA)	- 3Nos.
Voltmeter (0-10V)	- 3Nos.

KIRCHOFF'S CURRENT LAW:

The sum of the currents entering a junction is equal to the sum of the currents leaving the junction. In other words, if the current flowing towards a junction is taken as positive and the current flowing away from the junction is taken as negative, then this law states that the algebraic sum of all currents at a junction is zero.

KIRCHOFF'S VOLTAGE LAW:

The sum of the potential rises around any closed path in a circuit is equal to the sum of potential drops in it. In other words, the algebraic sum of the potential difference in a closed path is considered to be zero.

OHM'S LAW:

At constant temperature, the current flowing through the conductor is directly proportional to the potential difference applied across its ends.

V = I *R

PROBLEM:

Verify Kirchoff's current law at Junction A and voltage law in loop1 for the circuit shown in Figure.1

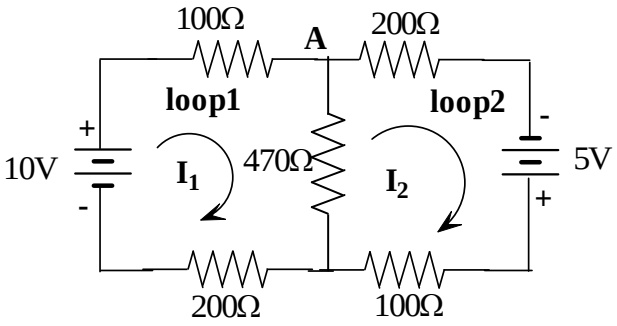


Figure.1

From the circuit, the loop equations are

For Loop1

$10 = 100I_1 + 470(I_1 - I_2) + 200I_1$

For Loop2

$5 = 470(I_2 - I_1) + 200I_2 + 100I_2$

Simplifying the equations, we get

$10 = 770I_1 - 470I_2$
$5 = -470I_1 + 770I_2$

Writing the above equations in the form of a matrix, we get

$$\begin{pmatrix} 770 & -470 \\ -470 & 770 \end{pmatrix}\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} 10 \\ 5 \end{pmatrix}$$

By applying crammer's rule

$$I_1 = \frac{\Delta_1}{\Delta}; I_2 = \frac{\Delta_2}{\Delta}$$

$$\Delta = \begin{vmatrix} 770 & -470 \\ -470 & 770 \end{vmatrix} = 372000$$

$$\Delta_1 = \begin{vmatrix} 10 & -470 \\ 5 & 770 \end{vmatrix} = 10050 \qquad \Delta_2 = \begin{vmatrix} 770 & 10 \\ -470 & 5 \end{vmatrix} = 8550$$

Now, I_1 = 27.02mA; I_2 = 22.98mA

Here I_1 and I_2 are the loop currents. From these, the branch currents I_3, I_4 and I_5 are found as follows:

$I_3 = I_1 = 27.02$ mA
$I_4 = I_2 = 22.98$ mA
$I_5 = I_1 - I_2 = 4.04$ mA

Here at node 'A', the current I_3 is the entering and I_4 & I_5 are leaving.

$I_3 = I_4 + I_5$
27.02 mA = 22.98 mA + 4.04 mA

Hence KCL is proved theoretically.

CIRCUIT DIAGRAM:

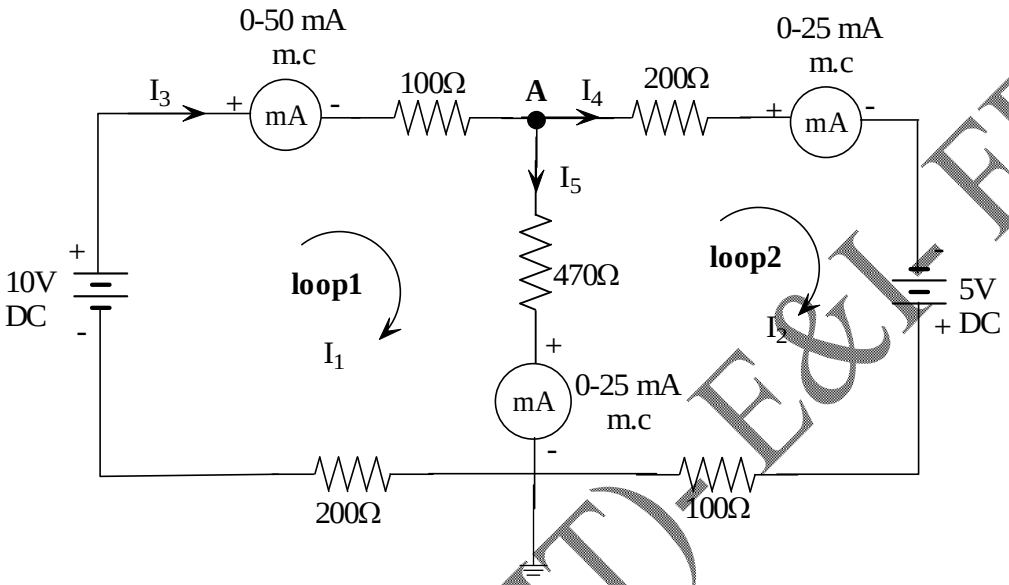


Figure.2 Practical Circuit to verify Kirchoff's Current Law

TABLE.1 VERIFICATION OF KIRCHOFF'S CURRENT LAW:

		Theoretical(mA)	**Practical (mA)**
Current through 100Ω	**$I_3 = I_1$(entering current)**	27.02	
Current through 200Ω	**$I_4 = I_2$(leaving current)**	22.98	
Current through 470Ω	**$I_5 = I_1 - I_2$(leaving current)**	4.04	

KIRCHOFF'S VOLTAGE LAW:

The sum of the potential rises around any closed path in a circuit is equal to the sum of potential drops in it. In other words, the algebraic sum of the potential difference in a closed path is considered to be zero.

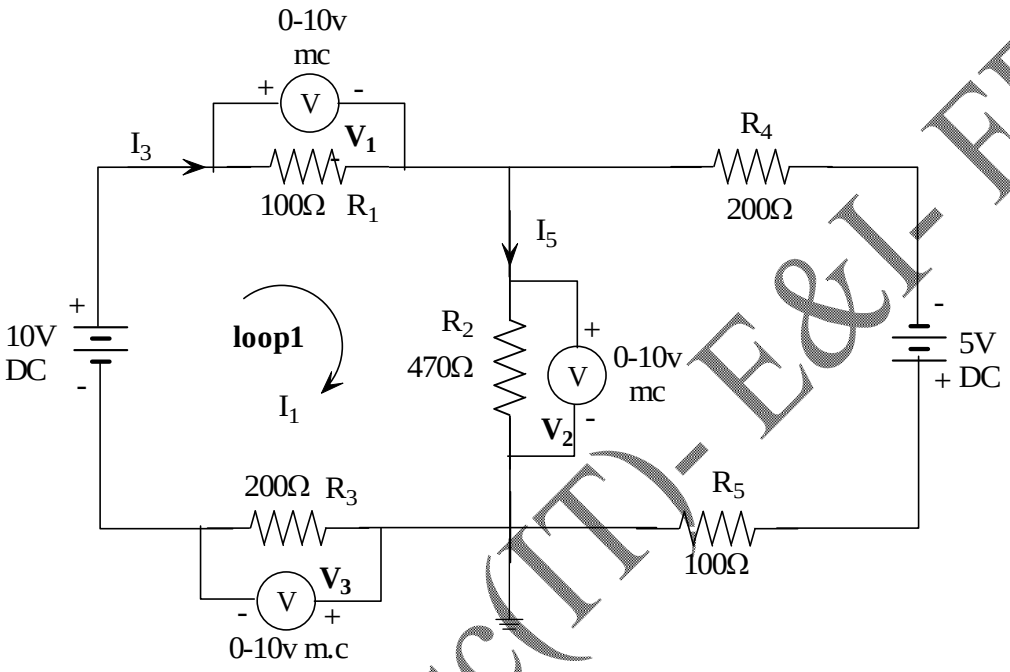


Figure.3 Practical Circuit to verify Kirchoff's Voltage Law

TABLE.2 VERIFICATION OF KIRCHOFF'S VOLTAGE LAW:

Element	Current through the resistance (mA)	Resistance value (Ω)	Voltage drop (Volts) Theoretical	Voltage drop (Volts) Practical
R_1	$I_1 = 27.02$	100	$V_1 = 2.702$	
R_2	$I_1 - I_2 = 4.04$	470	$V_2 = 1.899$	
R_3	$I_1 = 27.02$	200	$V_3 = 5.404$	

By KVL,

Sum of potential rise = Sum of potential drops

$V = V_1 + V_2 + V_3$

$10V = 2.702V + 1.899V + 5.404V$

$10V = 10V$

Hence KVL is verified.

OHM'S LAW:

From Figure.3, we measure the drop across the resistor R_1 i.e V_1

$$V_1 = I_1 * R_1$$
$$V_1 = 27.02 * 10^{-3} * 100\Omega$$
$$V_1 = 2.702 \text{volts}$$

TABLE.3 VERIFICATION OF OHM'S LAW:

Theoretical value of V_1 (V)	**Experimental value of V_1 (V)**
2.702	

PROCEDURE:

1. To verify Kirchoff's current law, make connections as shown in Figure.2.
2. Switch on the power supply, note down the ammeter readings and enter in the Table.1
3. Check whether the algebraic sum of currents is zero.
4. To verify Kirchoff's voltage law, make connections as shown in Figure.3.
5. Switch on the power supply, note down the voltmeter readings and enter in the
6. Check whether the algebraic sum of voltages is zero.
7. To verify ohm's law, make connections shown in Figure.3.
8. Switch on the power supply, note down V_1 and enter it in the Table.3
9. Compare the experimentally obtained V_1 with the theoretical V_1.

RESULT:

Thus the given DC circuit was analyzed and various laws were verified experimentally.

EXP NO:
DATE:

SIMULATION OF SUPER POSITION THEOREM AND TELLEGEN'S THEOREM USING ELECTRONIC WORK BENCH SOFTWARE

AIM:

To simulate and analyze super position theorem and tellegen's theorem using Electronic Work Bench software.

(A) SUPER POSITION THEOREM

THEOREM:

The current through, or voltage across, an element in a linear bilateral network is equal to the algebraic sum of the currents or voltages produced independently by each source.

THEORITICAL DETERMINATION OF I_L:

Figure 2 shows the given circuit considering the effect of E_1 (30V source)
To determine the current through R_L (1K) resistor i.e. I_{L1} when E_1 is present:
The total resistance of the network as seen by the source

$R_{T1} = R_1 + (R2 \,||\, RL) = 539.72\ \Omega$

The total current drawn by the network from the source

$I_{T1} = E_1/R_{T1} = 55mA.$

Applying current divider rule,

$I_2 = [R_2/ (R_2 + R_L)]\ I_{T1} = 17.58mA = I_{L1}$

Figure 3 shows the given circuit considering the effect of E_2 (10 V) source.

To determine the current through R_L (1K) resistor i.e. I_{L2} when E_2 is present:

The total resistance of the network as seen by the source

$R_{T2} = R_2 + (R_1 \,||\, RL) = 650\Omega$

The total current drawn by the network from the source

$I_{T2} = E_2/R_{T2} = 15.3mA.$

Applying current divider rule,

$I_2 = [R_1/ (R_1 + R_L)\ ]\ \ I_{T2} = 2.75mA = I_{L2}$

Total current through R_L,

$I_L = I_{L1} + I_{L2}$(Since I_{L1} and I_{L2} flow in the same direction)

$= 20.33mA.$

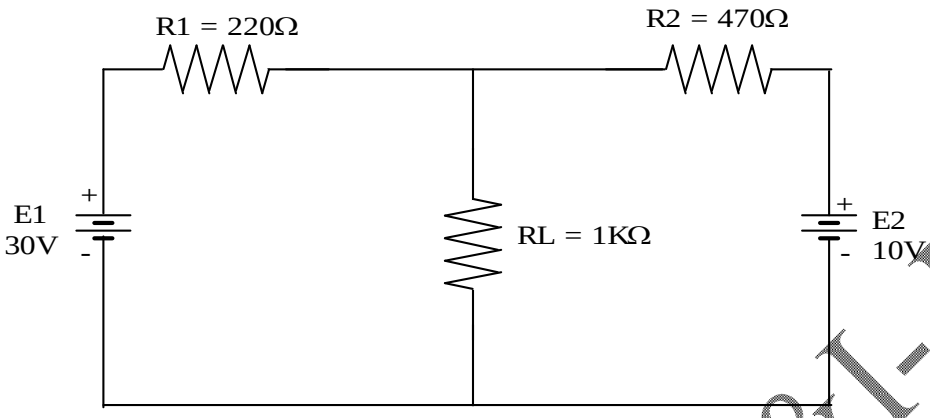


Figure.1 Given circuit

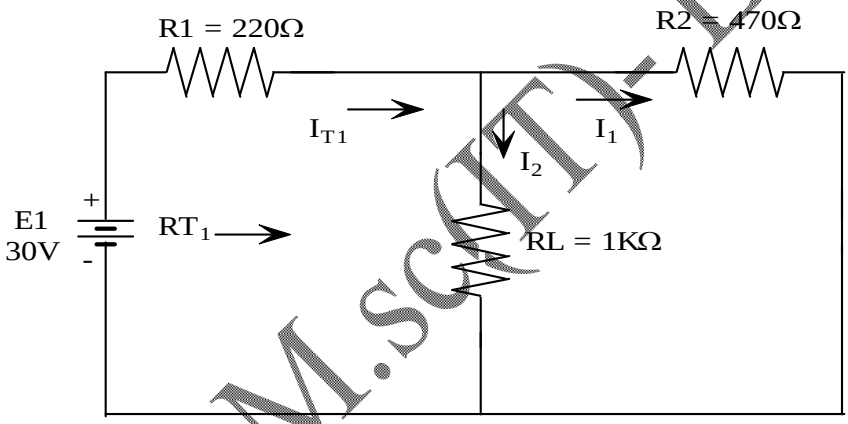


Figure.2 Considering the effect of E1 (30 V) source

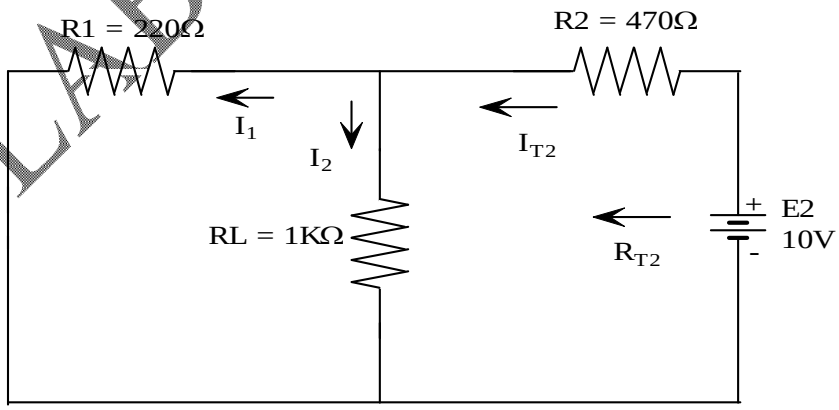


Figure.3 Considering the effect of E2 (10 V) source

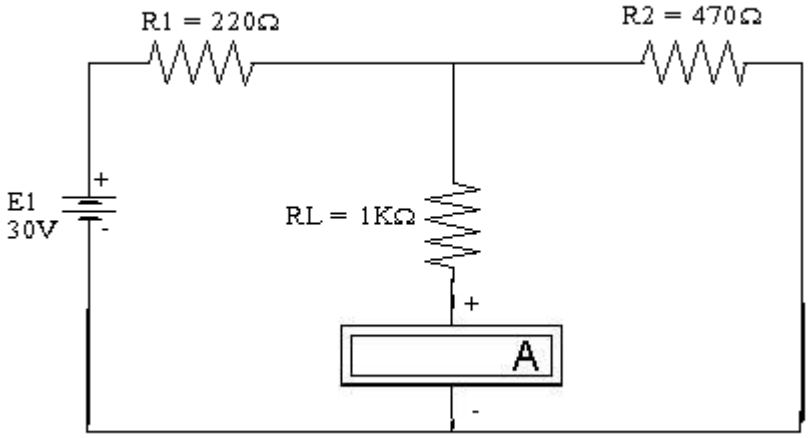


Figure.4 Connection diagram for determination of I_{L1}

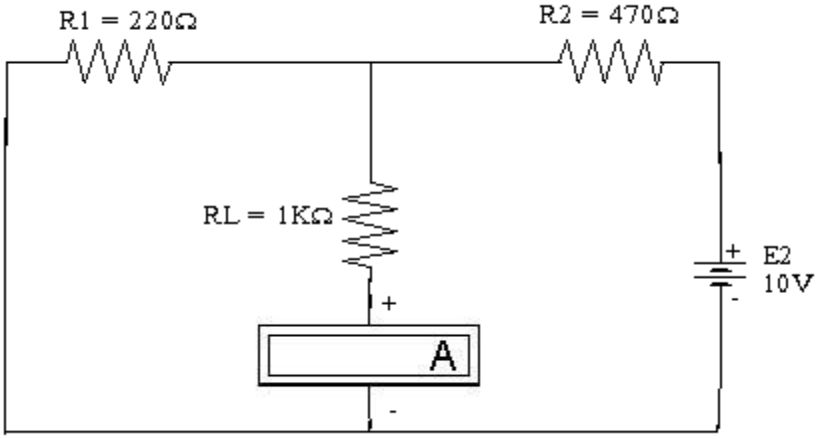


Figure.5 Connection diagram for determination of I_{L2}

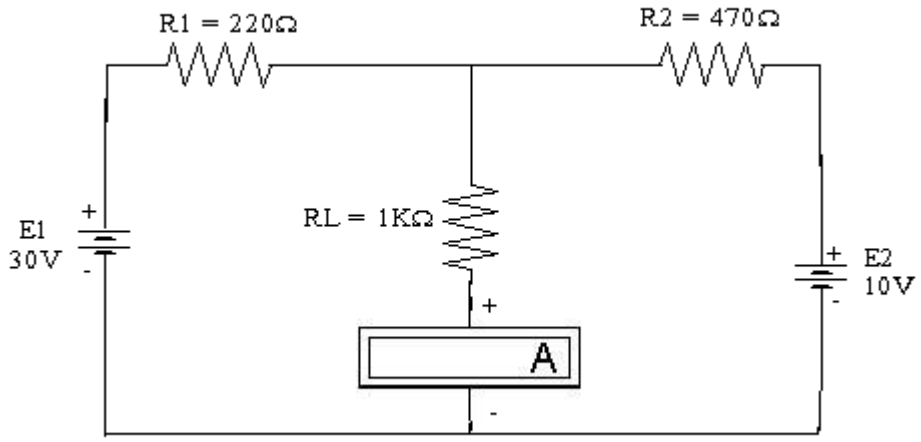


Figure.6 Connection diagram for determination of I_L

EXPERIMENTAL PROCEDURE FOR PRACTICAL DETERMINATION OF I_L:

1. Open the Electronic workbench software.
2. Choose the elements from the menu and give appropriate values.
3. Give connections as given in Figure 4, 5 & 6 by simply dragging the mouse.
4. To simulate the circuit, choose the **activate** option from analysis menu.
5. Verify the results and compare with theoretical values.

TABLE: VERIFICATION OF SUPERPOSITION THEOREM

Current	Theoretical value(mA)	Practical value(mA)
I_{L1}	17.58	
I_{L2}	2.75	
$I_L=I_{L1}+I_{L2}$	20.33	

(B) VERIFICATION OF TELLEGEN'S THEOREM

THEOREM:

For a given electrical network satisfying the Kirchhoff's law, the sum of the products of element current and the element voltage is zero.

THEORETICAL CALCULATION:

When 30V is supplied

Total resistance =470 || 1000 +220 =539.72Ω

By ohm's law ,

V= IR

I=V/R

I=30/539.72=0.055A

Current through 220 Ω = 0.055A

Current through 470 Ω = 0.0374A

Current through 1K Ω = 0.0175A

Voltage across 220 Ω = 12.1V

Voltage across 470 Ω = 17.57V

Voltage across 1K Ω = 17.57V

Voltage across source = 30V

VI = (30*0.055)+(17.57*0.0175)+(12.1*0.55)+(17.57*0.0374)

VI = 0.03 w

VI ≃0 w

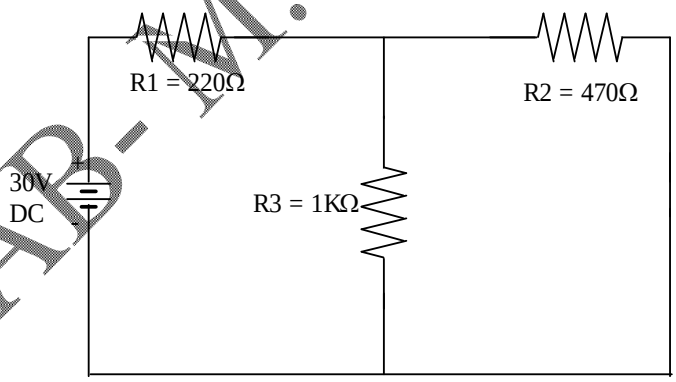


Figure.7 Given circuit diagram

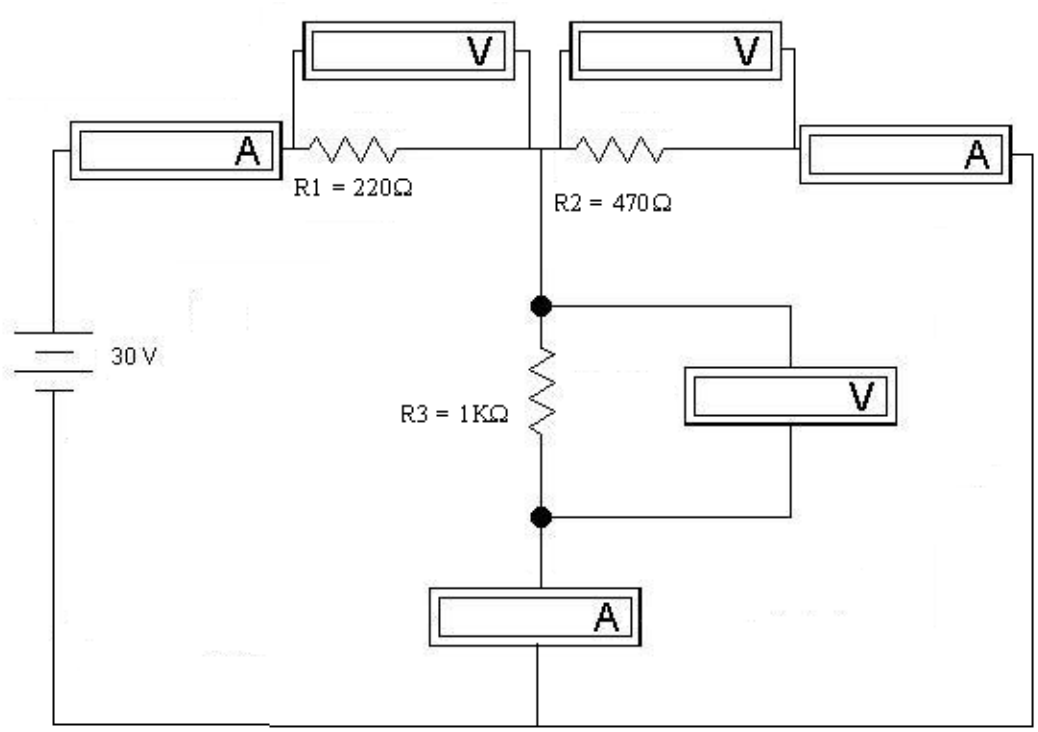


Figure.8 Circuit diagram to verify Tellegen's theorem

PROCEDURE:

1. Open the Electronic workbench software.
2. Choose the elements from the menu and give appropriate values.
3. Give connections as given in Figure 8 by simply dragging the mouse.
4. To simulate the circuit, choose the **activate** option from analysis menu.
5. Verify the results and compare with theoretical values.

TABULATION:

Element	Voltage(volts)		Current(A)		P = VI (watts)	
	Theoretical	Practical	Theoretical	Practical	Theoretical	Practical
220Ω Resistor	12.1		0.0550		0.6655	
1kΩ Resistor	17.57		0.0175		0. 3075	
470Ω Resistor	17.57		0.0374		0. 6571	
Source	**30V**					

Source Power = ……Watts

Absorbed Power by the resistors = ……Watts

RESULT:

The superposition theorem and Tellegen's theorem is studied and verified using EWB software.

EXP NO:
DATE:

SIMULATION OF SIMPLE ELECTRONIC CIRCUITS USING ELECTRONIC WORK BENCH SOFTWARE

AIM:

To simulate and analyze various simple operational amplifier based electronic circuits using work bench software.

THEORY:

An operational amplifier is a high gain direct coupled amplifier. The voltage gain can be controlled by externally providing the feedback. The operational amplifier can be used to perform a large number of mathematical operations by this passive feedback. It has two inputs and one output. The inputs are non - inverting and inverting terminals marked with ' + ' and ' - ' sign respectively.

Inverting Amplifier:

In this configuration the input signal is applied to the inverting terminal of the op-amp and the non - inverting terminal is connected to ground.

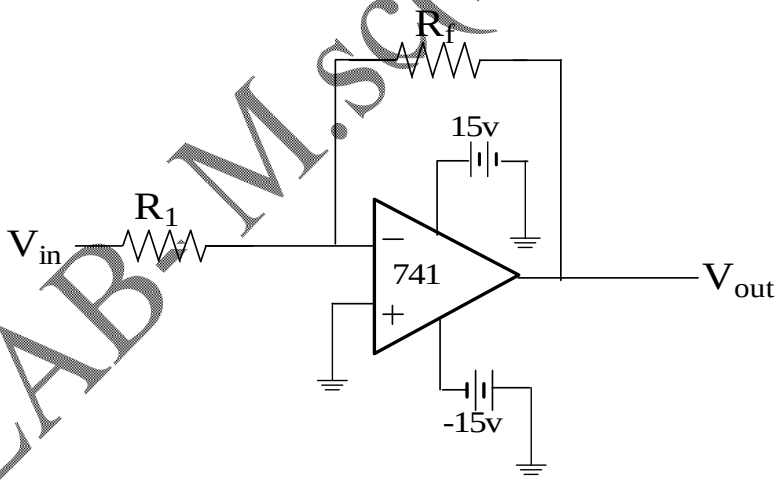


Figure.1 Inverting Amplifier

The output voltage of the inverting amplifier is given as

$$V_{out} = -\left(\frac{R_f}{R_1}\right)V_{in}$$

Here if $R_1 = 1K\Omega$ and $R_f = 10K\Omega$

$$V_{out} = -\left[\left(\frac{10K\Omega}{1K\Omega}\right)V_{in}\right] = -(10\,V_{in})$$

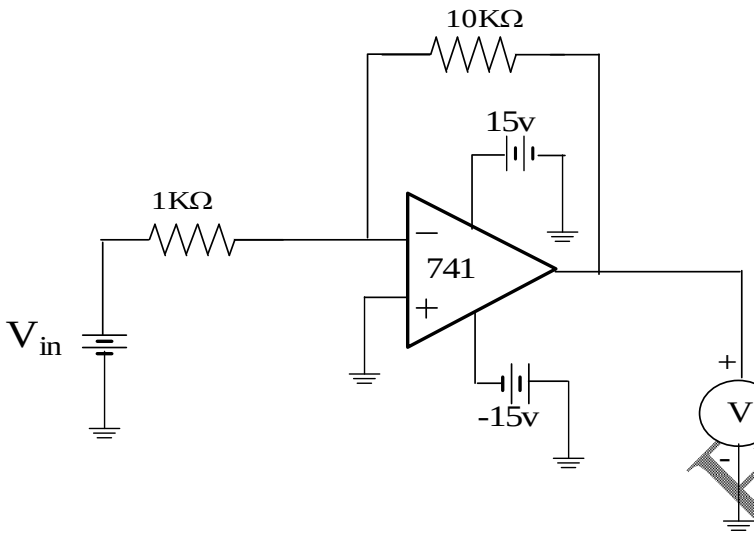


Figure.2 Practical circuit for Inverting Amplifier

TABULAR COLUMN:

V_{in}(volts)	V_{out}(volts)	Practical value (v)
0.5	-5	
0.2	-2	
1	-10	

Non Inverting Amplifier:

In this configuration the input signal is applied to the non - inverting terminal of the op-amp.

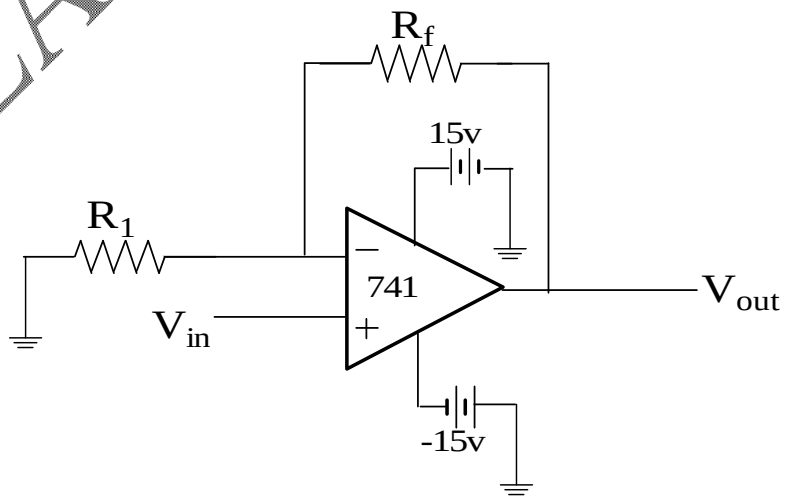


Figure.3 Non - Inverting Amplifier

The output voltage of the non-inverting amplifier can be given as

$$V_{out} = \left(1 + \frac{R_f}{R_1}\right) V_{in}$$

Here if $R_1 = 1K\Omega$ and $R_f = 1K\Omega$, then $V_{out} = \left[1 + \left(\frac{1K\Omega}{1K\Omega}\right)\right] V_{in} = (2V_{in})$

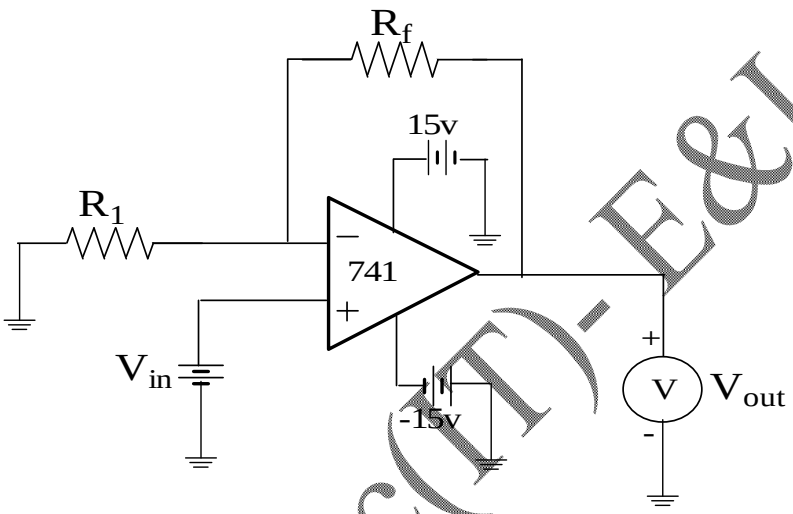


Figure.4 Practical circuit for Non - Inverting Amplifier

TABULAR COLUMN:

V_{in}(volts)	V_{out}(volts)	Practical value (v)
0.5	1	
0.2	0.4	
1	2	

Summer Amplifier:

This circuit sums the input voltages with suitable gain

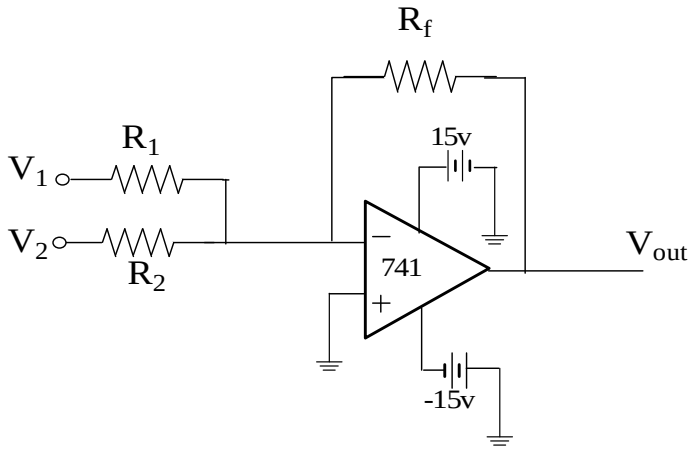


Figure.5 Summing Amplifier

The output voltage V_{out} can be written as

$$V_{out} = -\left[\left(\frac{R_f}{R_1}\right)V_1 + \left(\frac{R_f}{R_1}\right)V_2\right]$$

Here if R_1 =1KΩ, R_2 =1KΩ and R_f =1KΩ

$$V_{out} = -\left[\left(\frac{1K\Omega}{1K\Omega}\right)V_1 + \left(\frac{1K\Omega}{1K\Omega}\right)V_2\right] = -(V_1 + V_2)$$

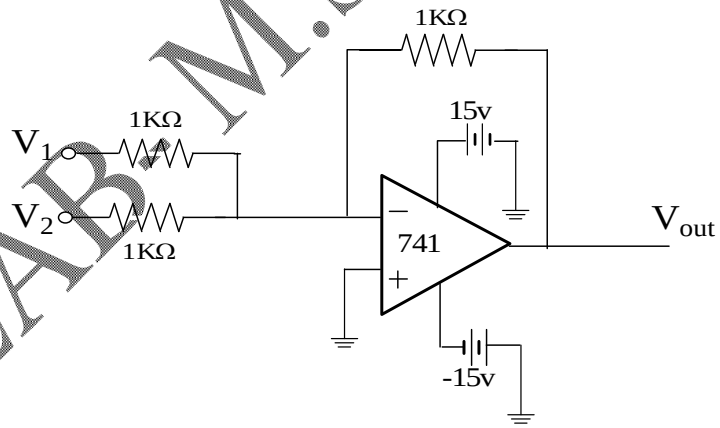


Figure.6 Practical circuit for Summing Amplifier

TABULAR COLUMN:

V_1(volts)	V_2(volts)	V_{out}(volts)	Practical value (volts)
1	2	-3	
2	1	-3	
2	-1	-1	

Voltage follower:

The output voltage follows the input voltage. The output of the voltage follower is given as

$V_{out} = V_{in}$

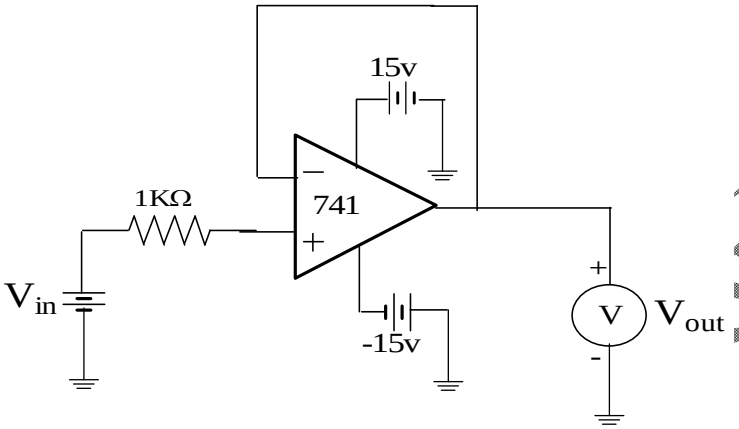


Figure.7 Practical circuit for Voltage follower

TABULAR COLUMN:

V_{in}(volts)	V_{out}(volts)	Practical values(v)
0.5	0.5	
5	5	
2	2	

Differential Amplifier:

The differential amplifier provides the output, which is the difference in input signals multiplied with gain.

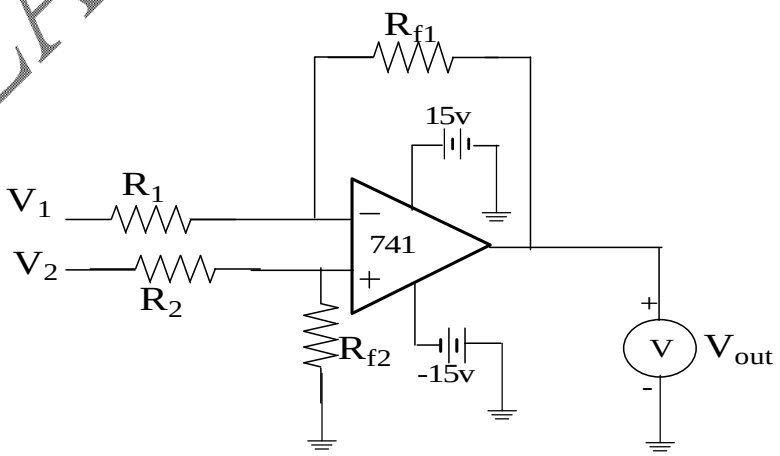


Figure.8 Differential Amplifier

The output voltage of the differential amplifier can be given as

$$V_{out} = \left[-\left(\frac{R_f}{R_1}\right)V_1 + \left(\frac{R_f}{R_1}\right)V_2 \right]$$

If $R_{f1} = R_{f2} = 1K\Omega$ and $R_1 = R_2 = 1K\ \Omega$

Then $$V_{out} = \left[-\left(\frac{1K\Omega}{1K\Omega}\right)V_1 + \left(\frac{1K\Omega}{1K\Omega}\right)V_2 \right] = -(V_1) + V_2$$

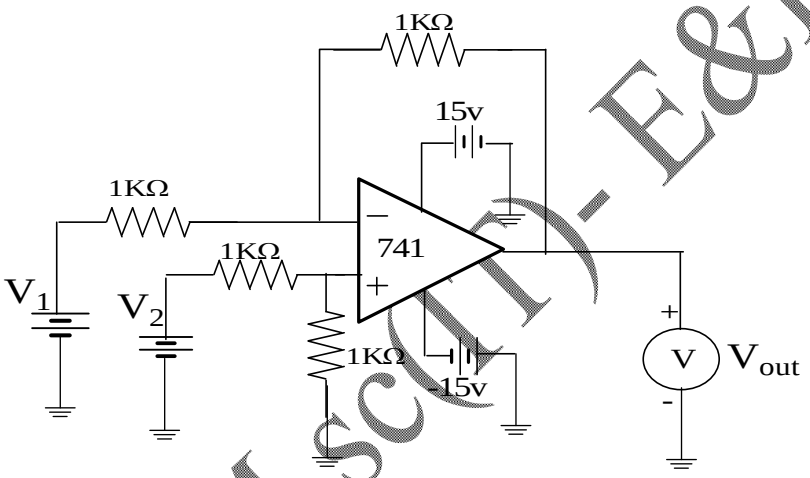


Figure.9 Practical circuit for Differential Amplifier

TABULAR COLUMN:

V_1(volts)	V_2(volts)	V_{out}(volts)	Practical values (v)
1	2	1	
2	1	-1	
2	-1	-3	

Comparator:

It is an open loop mode configuration of op-amp. Comparator compares the signal between the two terminals and produces positive or negative saturation.

Vout = +15V if $V_1 > V_2$
Vout = -15V if $V_2 > V_1$

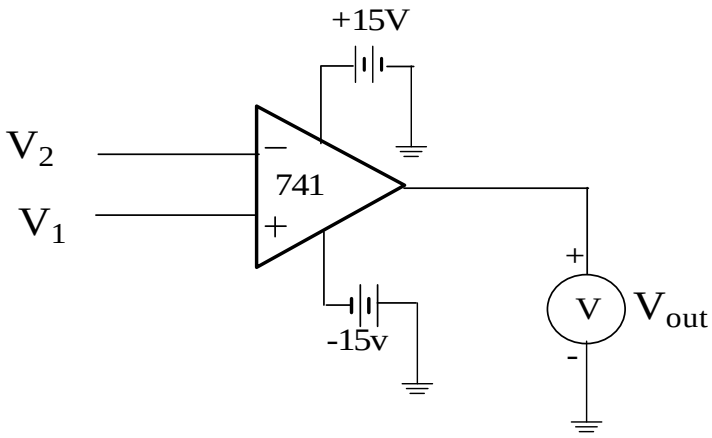


Figure.10 Practical circuit for Comparator

TABULAR COLUMN:

V_1(volts)	V_2(volts)	V_{out}(volts)	Practical values (v)
1	2	15	
2	1	15	
1	2	-15	

PROCEDURE:

6. Open the Electronic workbench software.
7. Choose the elements from the menu and give appropriate values.
8. Give connections by simply dragging the mouse.
9. To simulate the circuit, choose the **activate** option from analysis menu.
10. Verify the results.

RESULT:

Thus various applications of operational amplifier IC741 have been studied.

EXP NO:
DATE:

IMPLEMENTATION OF DIGITAL TO ANALOG CONVERTER USING MILLMAN'S THEOREM

AIM:

To design a 3-bit D/A converter using resistive divider network and verify practically.

COMPONENTS REQUIRED:

Digital Multimeter, Power Supply unit

THEORY:

Digital to Analog converters are used to convert digital input into analog output. Figure.1 shows the block diagram of 3-bit D/A converter. It has three input lines (D_2, D_1 and D_0) and one output line for the analog signal. The three input lines can assume eight ($2^3 = 8$) input combinations from 000 to 111(000, 001, 010, 011, 100, 101, 110, 111). D_2 is the most significant bit (MSB) and D_0 is the least significant bit (LSB).

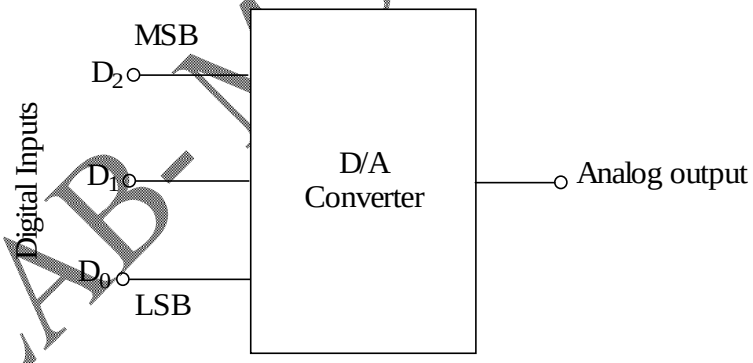


Figure.1 Block Diagram of 3-bit D/A Converter

A resistive divider network performs the D/A function as shown in Figure.2. Resistors R_0, $R_1$and R_2 form the divider network. Choose R_0, R_1 and R_2 should be such that

$$R_1 = \frac{R_0}{2}, \quad R_2 = \frac{R_0}{4}$$

The load resistor R_L should be large enough so that it does not load the divider network.

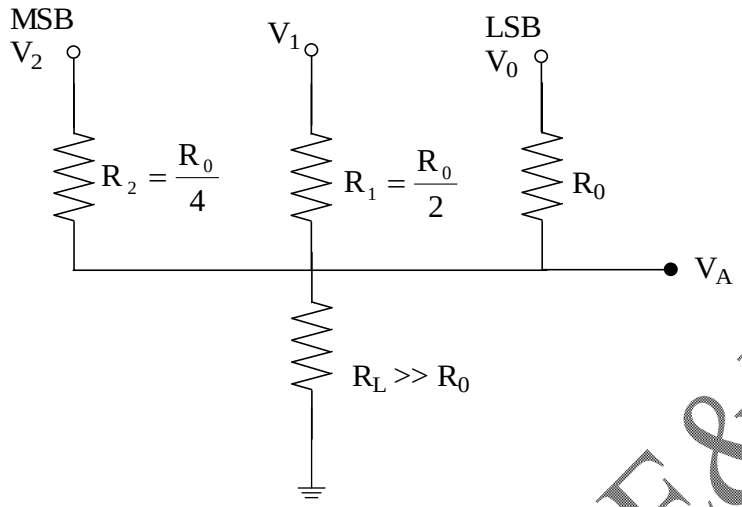


Figure.2 3-Bit Resistive Network

MILLMAN'S THEOREM:

The voltage appearing at any node in a resistive network is equal to the summation of the currents entering the node divided by the summation of conductance connected to that node.

In equation form analog voltage V_A is given as

$$V_A = \frac{\frac{V_0}{R_0} + \frac{V_1}{R_1} + \frac{V_2}{R_2} + ...}{\frac{1}{R_0} + \frac{1}{R_1} + \frac{1}{R_2} + ...}$$

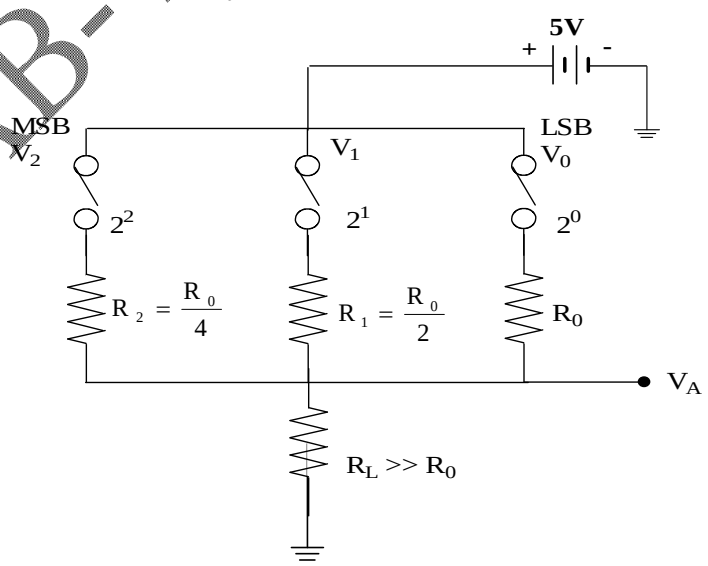


Figure.3 Resistive Divider Network

For the resistive divider network shown in Figure.3, applying Millman's theorem

$$\text{Analog Voltage } V_A = \frac{\frac{V_0}{R_0}+\frac{V_1}{R_1}+\frac{V_2}{R_2}}{\frac{1}{R_0}+\frac{1}{R_1}+\frac{1}{R_2}}$$

$$= \frac{\frac{V_0}{R_0}+\frac{V_1}{(R_0/2)}+\frac{V_2}{(R_0/4)}}{\frac{1}{R_0}+\frac{1}{(R_0/2)}+\frac{1}{(R_0/4)}}$$

$$= \frac{V_0+2V_1+4V_2}{1+2+4}$$

Rearranging, we get

$$\text{Ana log Voltage } V_A = \frac{4V_2+2V_1+V_0}{7}$$

For example, let **logic 0 = 0V, logic 1 = 5V**

For digital input **101**

$$\text{Ana log Voltage } V_A = \frac{4(5)+2(0)+1(5)}{7} = \frac{25}{7} = 3.571\text{volts}$$

MODIFIED MILLMAN'S THEOREM:

The analog voltage V_A can also be determined for any of the digital input data by using the modified form of Millman's theorem given as

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + ... + V_{n-1} 2^{n-1}}{2^{n-1}}$$

Where V_0, V_1, V_2… V_{n-1} is the digital input voltage levels and n is the number of input bits. For the 3-bit network

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2}{2^{3-1}}$$

Rearranging, we get

$$V_A = \frac{V_2 2^2 + V_1 2^1 + V_0 2^0}{2^{3-1}}$$

For example, let **logic 0 = 0V, logic 1 = 5V**

For digital input **1 0 1**

$$\text{Analog Voltage } V_A = \frac{(5)2^2 + (0)2^1 + (5)2^0}{2^{3-1}} = \frac{25}{7} = 3.571\text{volts}$$

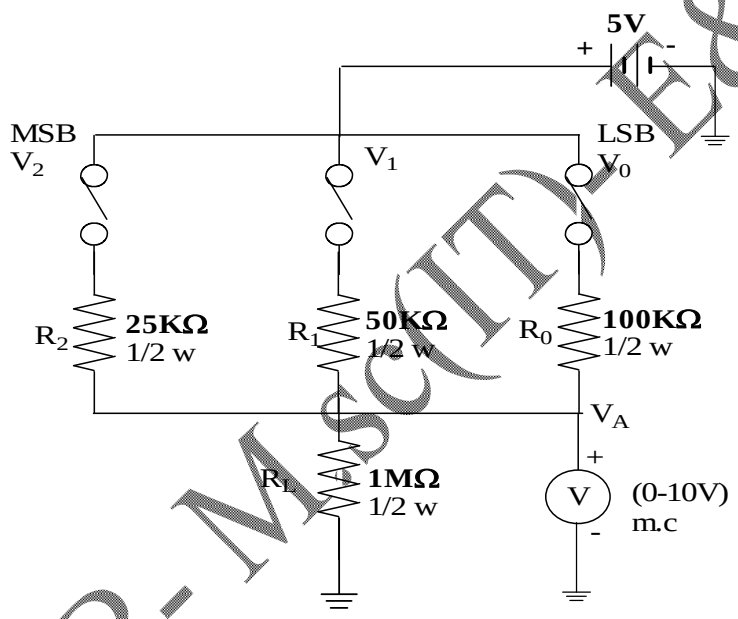


Figure.4 Practical Circuit for 3-Bit D/A Converter

PROCEDURE:

1. Give connection as per the circuit diagram shown in Figure.4
2. Assume, **logic 0 = 0V, logic 1 = 5V**
3. Predetermine the analog output values for different input combinations
4. Give the different digital input combinations (**logic 0 = 0V, logic 1 = 5V)** and verify the analog output using the multimeter.

PREDETERMINATION OF ANALOG VOLTAGES:

For digital input 000

$$V_A = \frac{(0)2^2 + (0)2^1 + (0)2^0}{2^{3-1}} = \frac{0}{7} = 0\text{volts}$$

For digital input 001

$$V_A = \frac{(0)2^2 + (0)2^1 + (5)2^0}{2^{3-1}} = \frac{5}{7} = 0.714\text{volts}$$

For digital input 111

$$V_A = \frac{(5)2^2 + (5)2^1 + (5)2^0}{2^{3-1}} = \frac{35}{7} = 5\text{volts}$$

TABULAR COLUMN:

Digital Input			**Analog Output**	
V_2	V_1	V_0	Predetermined output (volts)	Observed output (volts)
0	**0**	**0**	0	
0	**0**	**1**	0.714	
0	**1**	**0**	1.428	
0	**1**	**1**	2.142	
1	**0**	**0**	2.857	
1	**0**	**1**	3.571	
1	**1**	**0**	4.285	
1	**1**	**1**	5.000	

Result:

Thus a 3-bit D/A converter have been designed and its analog voltage is verified for different digital input combinations.

EXP NO:
DATE:

MULTIPLEXER AND DEMULTIPLEXER

AIM:

To verify the truth table of digital multiplexer using IC 74150 and digital demultiplexer using IC 74154.

COMPENENTS REQUIRED:

5V power supply unit, Digital multiplexer(IC 74150),
Digital demultiplexer(IC 74154) and Digital multimeter.

A) MULTIPLEXER

THEORY:

Multiplexer means many into one. Multiplexer is a circuit with many inputs but only one output. The general block diagram of multiplexer is shown in Figure.2 by applying suitable control signal we can steer any input to the output. The circuit has "n" input signals ,"m" control signals and 1 output signal. The input bits are labeled as D_0 to $D_{15,}$ control signals as A,B,C,D & output bit as Y.

The IC 74150 is a 16 to 1 multiplexer with the pin diagram as shown in Figure.1
The expression for multiplexer output is given as $Y= D_n$

Where n is the decimal equivalent of ABCD. A low state enables the multiplexer and output is equal to the complement of the input data bit.

A high strobe disables the multiplexer and forces the output into the high state.

PROCEDURE:

1. Form the truth table as in Table.1
2. Apply the input and control signals as in Table.1
3. Verify the output using voltmeter.

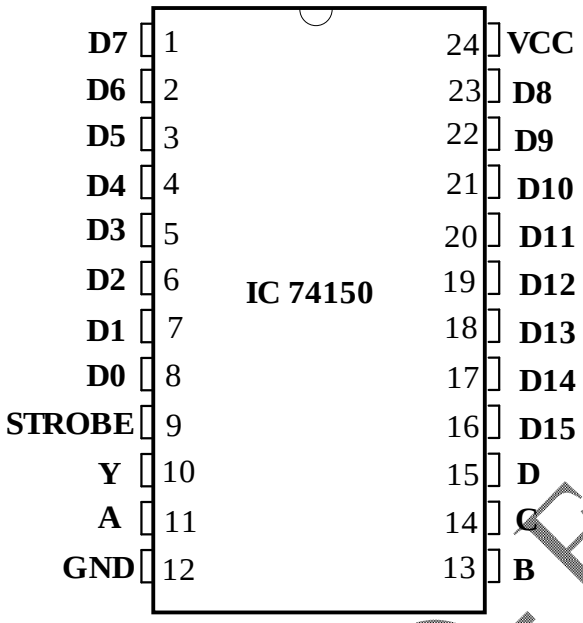


Figure.1 Pin Diagram of Digital Multiplexer

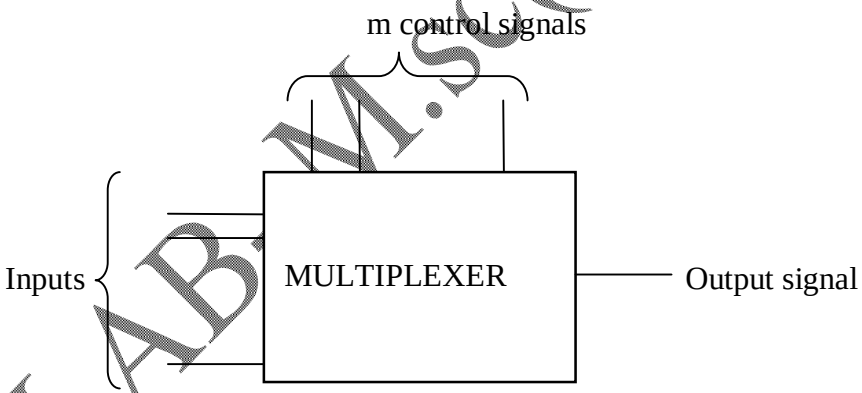


Figure.2 General Block Diagram of Multiplexer

Table 1 - Truth Table of Multiplexer [IC 74150]

A	B	C	D	STROBE	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	Y	o/p (v)
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	
0	0	0	1	0	X	O	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0	
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1	
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0	
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1	
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0	
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1	
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0	
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1	
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0	
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1	
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0	
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1	
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0	
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1	
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0	
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1	
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0	
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1	
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0	
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1	
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0	
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1	
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0	
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1	
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0	
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	

B) DEMULTIPLEXER

THEORY :

Demultiplexing means one to many. Demultiplexer is a logic circuit with one input and many outputs. By applying control signal we can steer the input signal to one of the output lines. The general block diagram of the demultiplexer is shown in Figure.4.

74154 is a 4 to 16 decoder which provides decoding of four bit binary coded input into one of mutually exclusive outputs when both the strobe inputs E1 & E2 are in the zero state. Each of the strobe input can be used as data input to perform the demultiplexer function by using the 4 input lines to address the output line and having the other strobe input zero. When either of the strobe signal is high all outputs are high.

PROCEDURE:

1. Form the truth table as in Table.2.
2. Apply the input and control signals as in Table.2
3. Verify the output using voltmeter.

Table 2 Truth Table of Demultiplexer [IC 74154]

STROBE	DATA	D	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{14}	Q_{15}
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Practical Values from voltmeter

Logic 0	
Logic 1	

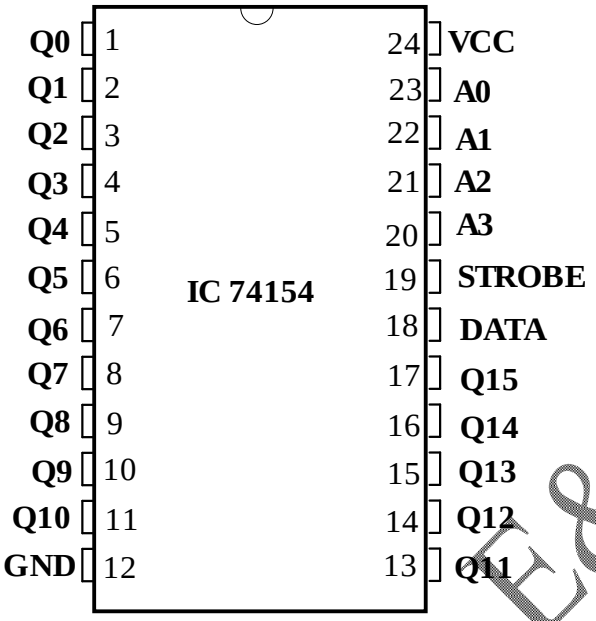


Figure.3 Pin Diagram of Digital De multiplexer

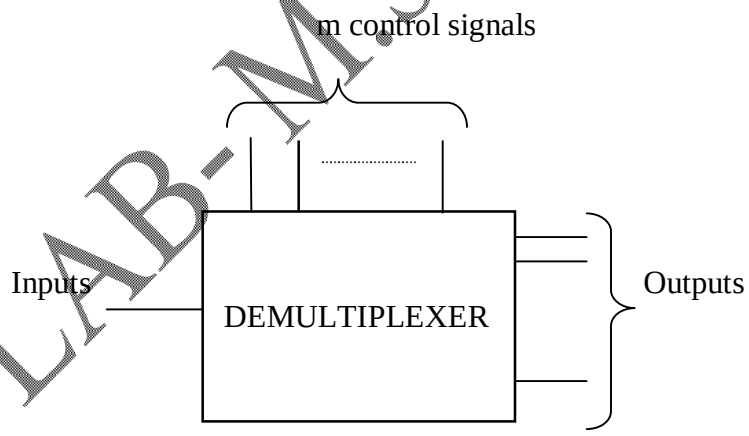


Figure.4 General Block Diagram of Demultiplexer

RESULT:

The truth table of the digital multiplexer using IC 74150 and the digital demultiplexer using IC 74154 was verified.

EXP NO:
DATE:

VERIFICATION OF LOGIC GATES USING INTEGRATED CHIPS

AIM:

To construct the basic gates AND, OR, NOT, NAND, EX-OR and NOR and verify their truth table.

APPARATUS REQUIRED:

IC7400 -	NAND Gate	-	1 No
IC7402 -	NOR Gate	-	1 No
IC7404 -	NOT Gate	-	1 No
IC7408 -	AND Gate	-	1 No
IC7432 -	OR Gate	-	1 No
IC7486 -	EX-OR Gate	-	1 No

PROCEDURE:

(i) AND GATE

The expression for two input AND gate is A.B. Connect pin 14 to +5V DC and pin 7 to GND. Use +5V for logic 1 and 0V for logic 0. Verify the output for various combinations of the input, with the truth table of the AND gate given in Table.1. The pin detail of IC7408 is shown in Figure.1.

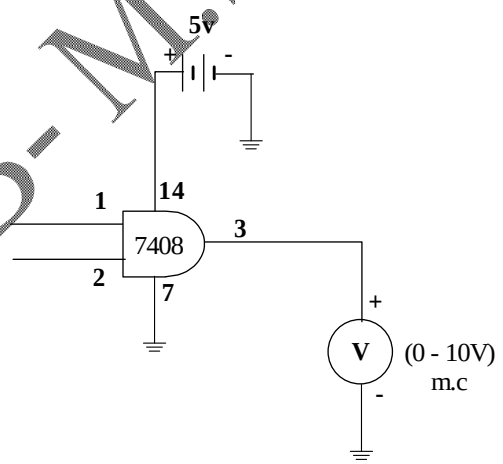


Figure.1 Practical Circuit for verification of AND Gate

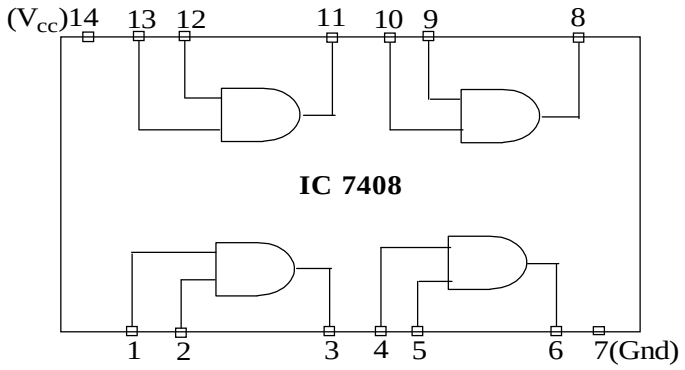


Figure.2 Pin Detail of IC 7408(AND gate)

Table.1. Truth Table for AND Gate

A	B	Y=A.B	Practical Value in Volts
0	0	0	
0	1	0	
1	0	0	
1	1	1	

(ii) OR GATE

The expression for two input OR gate is A+B. Connect pin 14 to +5V DC and pin 7 to GND. Use +5V for logic 1 and 0V for logic 0. Verify the output for various combinations of the input, with the truth table of the OR gate given in Table.2. The pin detail of IC7432 is shown in Figure.3.

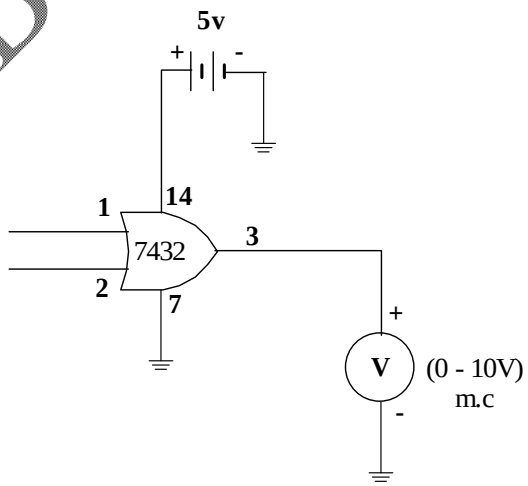


Figure.3 Practical Circuit for verification of OR Gate

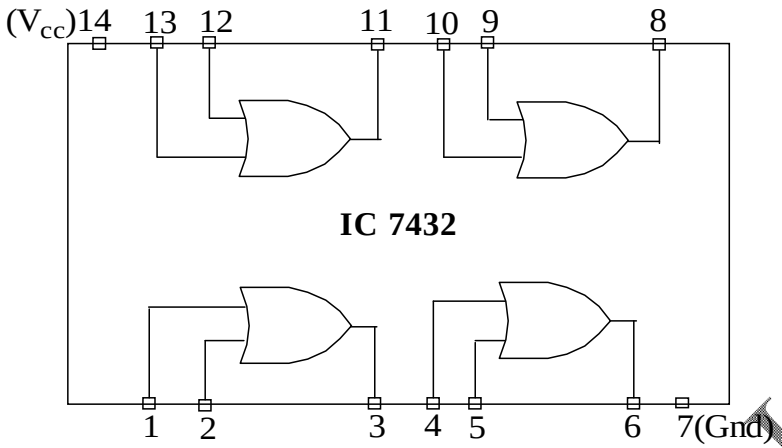


Figure.4 Pin Detail of IC 7432(OR gate)

Table.2. Truth Table for OR Gate

A	B	Y=A+B	Practical Value in Volts
0	0	0	
0	1	1	
1	0	1	
1	1	1	

(iii) NAND GATE

The expression for two input NAND gate is $\overline{A.B}$. Connect pin 14 to +5V DC and pin 7 to GND. Use +5V for logic 1 and 0V for logic 0. Verify the output for various combinations of the input, with the truth table of the NAND gate given in Table.3. The pin detail of IC7400 is shown in Figure.5.

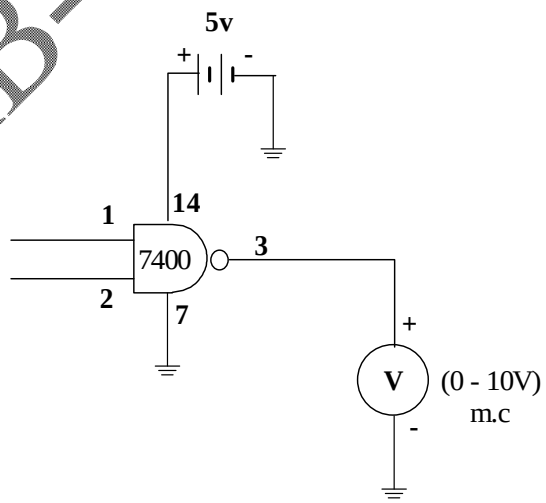


Figure.5 Practical Circuit for verification of NAND Gate

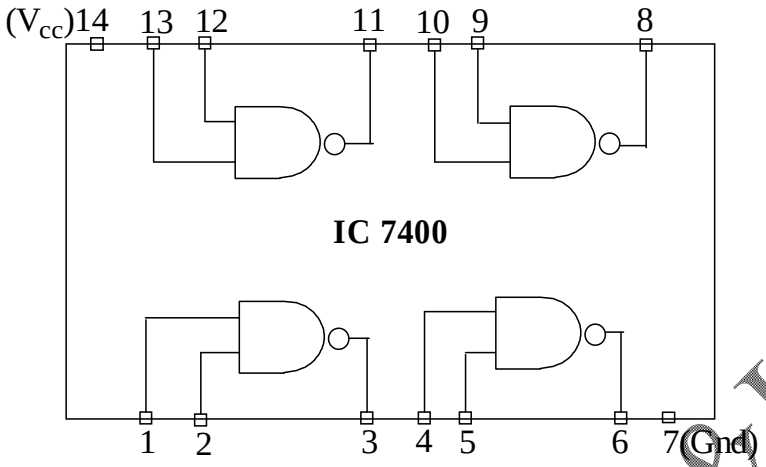


Figure.6 Pin Detail of IC 7400(NAND gate)

Table.3. Truth Table for NAND Gate

A	B	Y= $\overline{AB}$	Practical Value in Volts
0	0	1	
0	1	1	
1	0	1	
1	1	0	

(iv) NOR GATE

The expression for two input NOR gate is $\overline{A+B}$. Connect pin 14 to +5V DC and pin 7 to GND. Use +5V for logic 1 and 0V for logic 0. Verify the output for various combinations of the input, with the truth table of the NOR gate given in Table.4. The pin detail of IC7402 is shown in Figure.7.

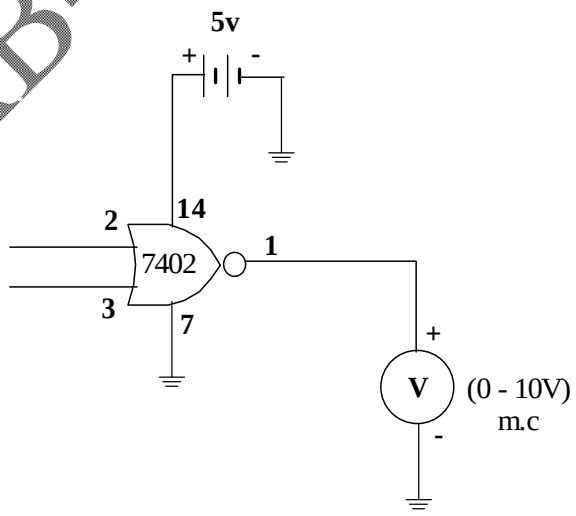


Figure.7 Practical Circuit for verification of NOR Gate

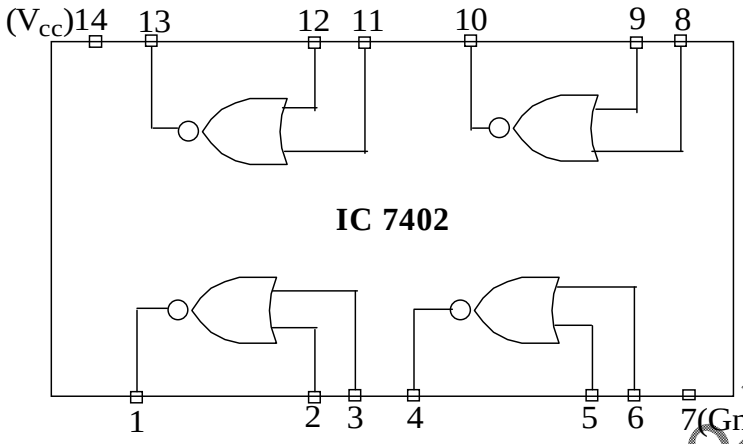


Figure.8 Pin Detail of IC 7402(NOR gate)

Table.4. Truth Table for NOR Gate

A	B	Y= $\overline{A+B}$.	Practical Value in Volts
0	0	1	
0	1	0	
1	0	0	
1	1	0	

(v) NOT GATE

The expression for two input NOT gate is $\overline{A}$. Connect pin 14 to +5V DC and pin 7 to GND. Use +5V for logic 1 and 0V for logic 0. Verify the output for various combinations of the input, with the truth table of the NOT gate given in Table.5. The pin detail of IC7404 is shown in Figure.9.

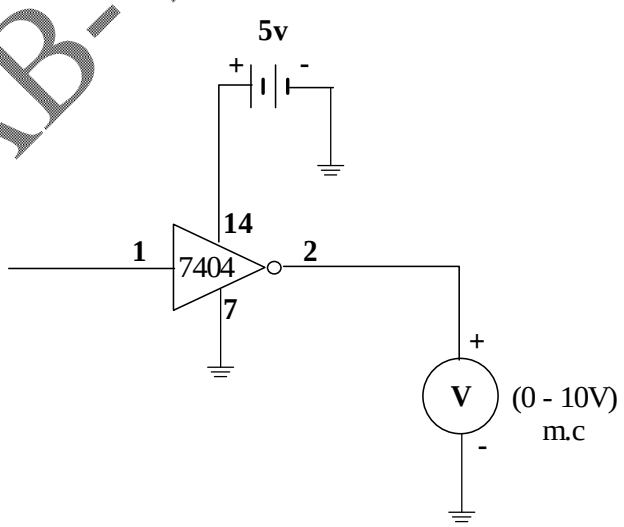


Figure.9 Practical Circuit for verification of NOT Gate

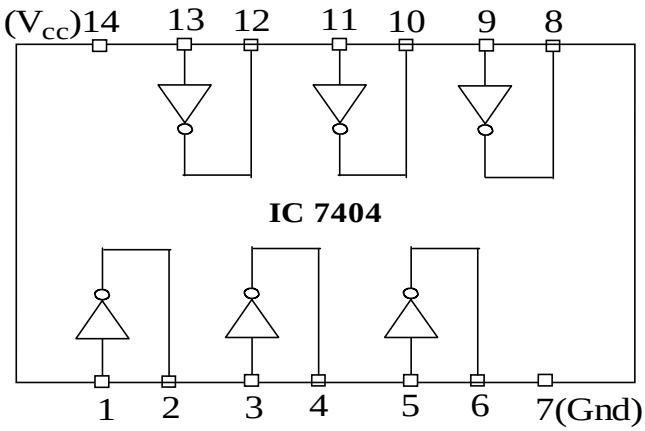


Figure.10 Pin Detail of IC 7404(NOT gate)

Table.5. Truth Table for NOT Gate

A	Y= $\overline{A}$	Practical Value in Volts
0	1	
1	0	

(vi) EX-OR GATE

The expression for two input EX-OR gate is $A \oplus B$. Connect pin 14 to +5V DC and pin 7 to GND. Use +5V for logic 1 and 0V for logic 0. Verify the output for various combinations of the input, with the truth table of the EX-OR gate given in Table.6. The pin detail of IC7486 is shown in Figure.6.

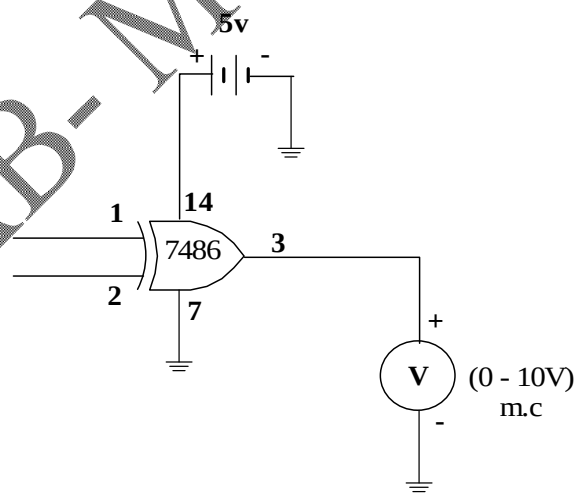


Figure.11 Practical Circuit for verification of EX-OR Gate

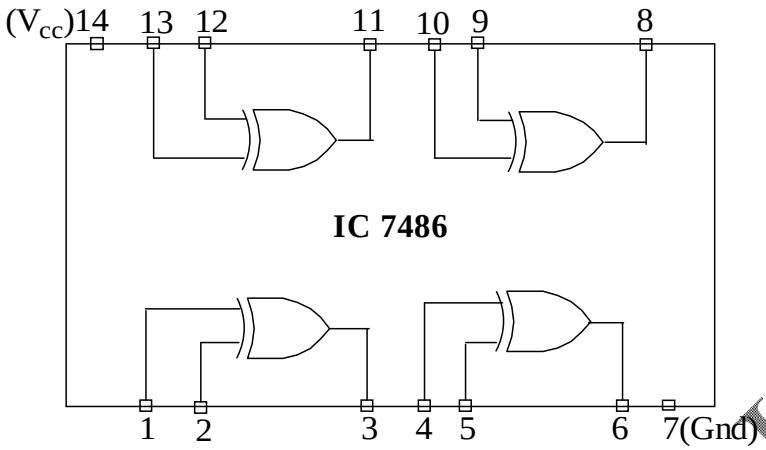


Figure.12 Pin Detail of IC 7486(XOR gate)

Table.6. Truth Table for EX-OR Gate

A	B	Y= A⊕ B	Practical Value in Volts
0	0	0	
0	1	1	
1	0	1	
1	1	0	

Result:

Thus truth table of various logic gates has been verified.

EXP NO:
DATE:

IMPLEMENTATION OF HALF ADDER AND HALF SUBTRACTOR USING LOGIC GATES

AIM:

To construct and verify the operation of the half adder and half subtractor circuits using suitable logic gates.

COMPONENTS REQUIRED:

IC 7486 - (Ex-Or gate) -1 NO.
IC 7408 - (AND gate) -1 NO.
IC 7432 - (OR gate) -1 NO.
IC 7404 – (NOT gate) -1 NO.
Voltmeter (0-10v)

THEORY:

The most basic arithmetic operation is the addition of two binary digits. This simple addition consists of four possible elementary operations: 0 + 0 = 0, 0 + 1 = 1, 1 +0 = 1 and 1 + 1 = 10. The first three operations produce a sum of one digit, but the last operation produce the binary sum of two digits. The higher significant bit of the result is called as carry. A combinational circuit that performs addition of two bits is called a Half Adder and the circuit that performs subtraction of two bits is called a Half Subtractor.

(A)HALF ADDER

This circuit needs two binary input and two binary outputs. The input variables designate the augend and addend bits and output variables produce the sum and the carry. We assign symbols A and B to the inputs and Sum and Carry to the outputs. The Carry output is 0 unless both the inputs are 1. The Sum output represents the least significant bit of the sum. The truth table is shown in Table.1

Table.1. Truth table for Half Adder operation

BINARY INPUTS		BINARY OUTPUTS	
A	**B**	**SUM**	**CARRY**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(B) HALF SUBTRACTER

This circuit needs two binary input and two binary outputs. The input variables denoted by A and B and the output variables are D(difference) and B(borrow). The truth table is shown in Table.2

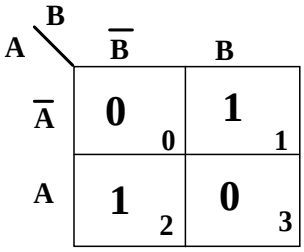
Table.2. Truth table for Half Subtractor operation

BINARY INPUTS		BINARY OUTPUTS	
A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

KARNAUGH MAP FOR HALF ADDER AND HALF SUBTRACTOR:

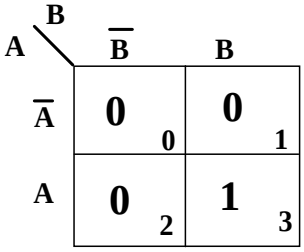
Half Adder:

Sum Map



$$Sum = \overline{A}B + A\overline{B}$$
$$= A \oplus B$$

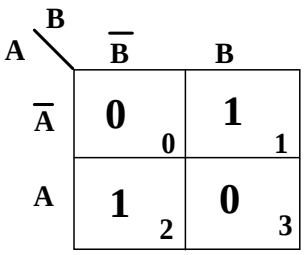
Carry Map



$$Carry = A.B$$

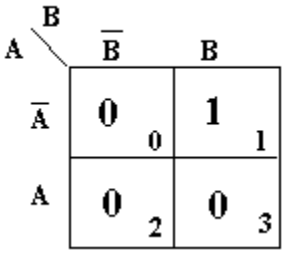
Half Subtractor:

Difference Map



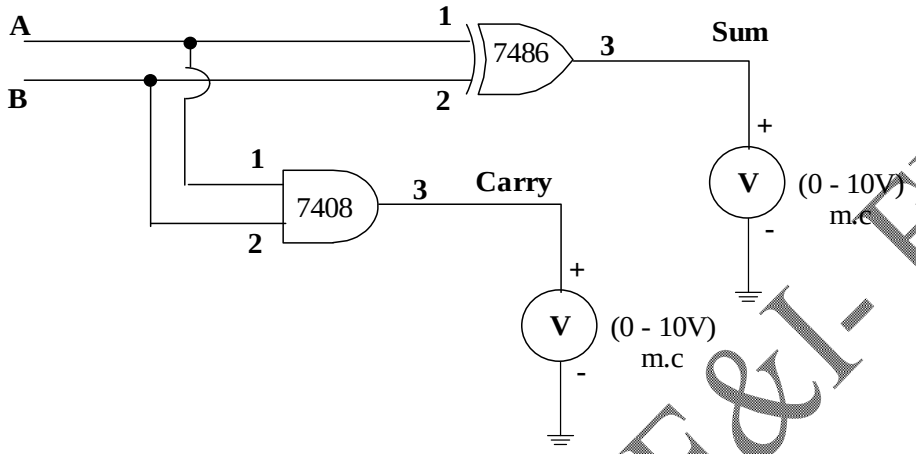
$$Difference = \overline{A}B + A\overline{B}$$
$$= A \oplus B$$

Borrow Map



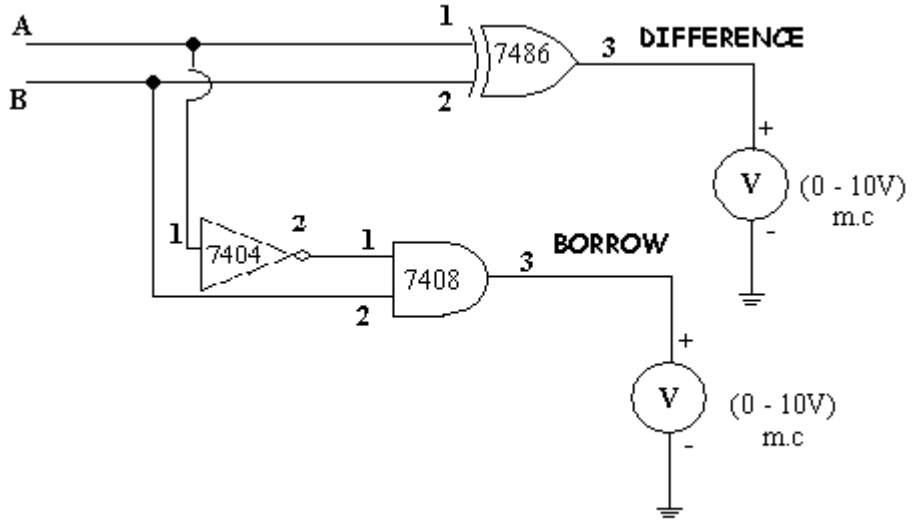
$$Borrow = \overline{A}B$$

CIRCUIT DIAGRAM:



For IC's 7486 and 7408 connect pin 14 to +5v DC and pin 7 to Grd

Figure.1. Circuit diagram of Half-Adder



For IC's 7486, 7404 and 7408 connect pin 14 to +5v and pin 7 to Grd

Figure.2. Circuit diagram of Half-Subtractor

PROCEDURE:

(A)HALF ADDER

1. Using logic expression given in the equation, build the circuit for a half adder using suitable gates as shown in Figure.1.

2. Verify the half adder operation for various input combinations and tabulate the voltmeter reading in Table.3.

Table.3. Tabular column to verify Half Adder Circuit

Binary Inputs		Binary Outputs		Practical value (volts)	
A	B	SUM	CARRY	SUM	CARRY
0	0	0	0		
0	1	1	0		
1	0	1	0		
1	1	0	1		

logic 0 = 0V, logic 1 = 5V

(B) HALF SUBTRACTOR

1. Using logic expression given in the equation, build the circuit for a half subtractor using suitable gates as shown in Figure.2.
2. Verify the half subtractor operation for various input combinations and tabulate the voltmeter reading in Table.4.

Table.4. Tabular column to verify Half Subtractor Circuit

Binary inputs		Binary outputs		Practical values (volts)	
A	B	Difference	Borrow	Difference	Borrow
0	0	0	0		
0	1	1	1		
1	0	1	0		
1	1	0	0		

Table.4. Tabular column to verify Full Adder Circuit

logic 0 = 0V, logic 1 = 5V

RESULT

Thus the half adder and half subtractor circuits were verified experimentally.

EXP NO:
DATE:

SIMPLIFICATION OF LOGIC EXPRESSIONS USING KARNAUGH MAP TECHNIQUES

AIM:

To realize the given logic functions using suitable gates.

$F1 = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,\overline{D} + A\,B\,C\,\overline{D}$

$F2 = \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}\,B\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,D + A\,B\,C\,D$

with don't cares

$d = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,B\,C\,\overline{D}$

$F3 = \left(\overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D} + A\,B\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,\overline{B}\,\overline{C}\,\overline{D}\right) * \left(A\,\overline{C} + C\right)$

COMPONENTS REQUIRED:

IC 7486-XOR gate, IC 7408-AND gate, Regulated power supply and 0-10V range voltmeter.

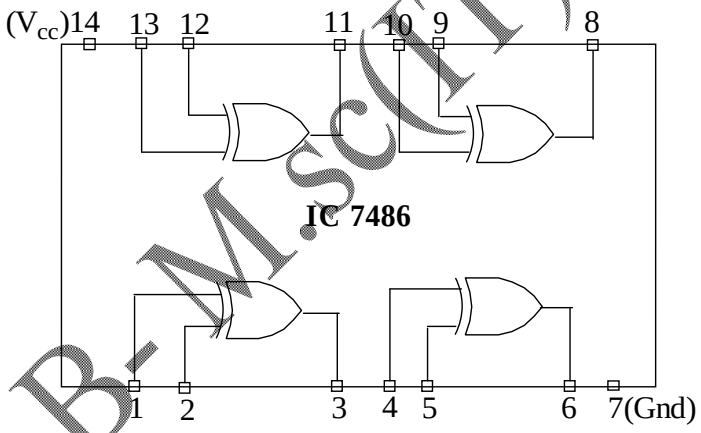


Figure.1 Pin Diagram of IC 7486

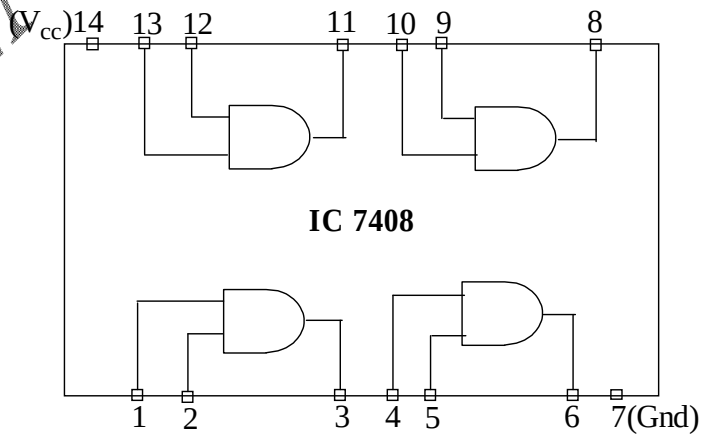


Figure.2 Pin Diagram of IC 7408

SOLUTION:

Function F1

$$F1 = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,\overline{D} + A\,B\,C\,\overline{D}$$

The function F1 is given in sum of minterms, which can be expressed as

$$F1 = \sum m(1,3,4,6,9,11,12,14)$$

Since the number of variables involved is four, the given minterms are mapped using the four variable map and grouping all the ones, there are two quad groups as shown in Figure.3

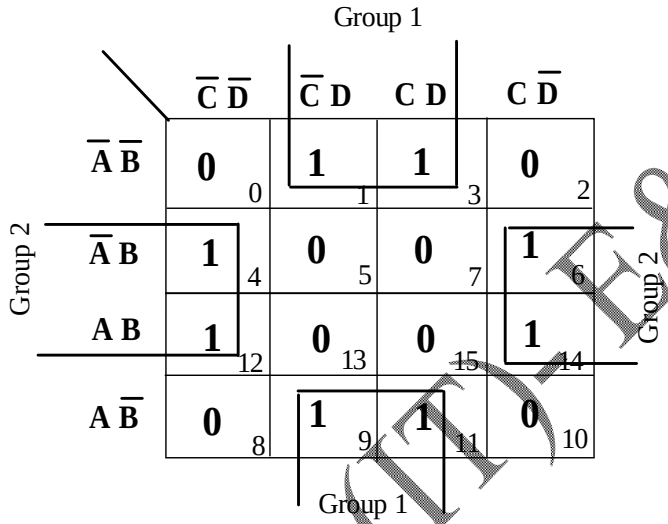


Figure.3 K-map of Function F1

From the map

Group Number	Minterms involved	Reduced to
Group I	1, 3, 9, 11	$\overline{B}\,D$
Group II	4,6,12,14	$B\,\overline{D}$

Hence F1 is reduced to

$$F1 = \overline{B}\,D + B\,\overline{D} = B \oplus D$$

Which implies the XOR function that can be implemented using one of the four gates in IC 7486 as shown in Figure.4

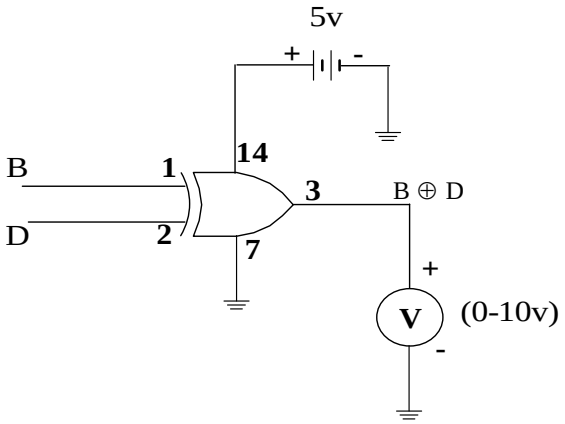


Figure.4 Implementation of Function F1 using IC 7486

TABULAR COLUMN:

B	D	B ⊕ D	Practical Value of F1 in volts
0	0	0	
0	1	1	
1	0	1	
1	1	0	

Function F2

$F2 = \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}\,B\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,D + A\,B\,C\,D$

with don't cares

$d = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,B\,C\,\overline{D}$

$F2 = \sum m(2,4,9,11,13,15) \quad d = \sum m(0,6)$

Function F2 has sum of minterms and don't cares with four variables. Using Karnaugh map it is mapped and grouping all the ones with possible don't cares, there are two quad groups as shown in Figure.5

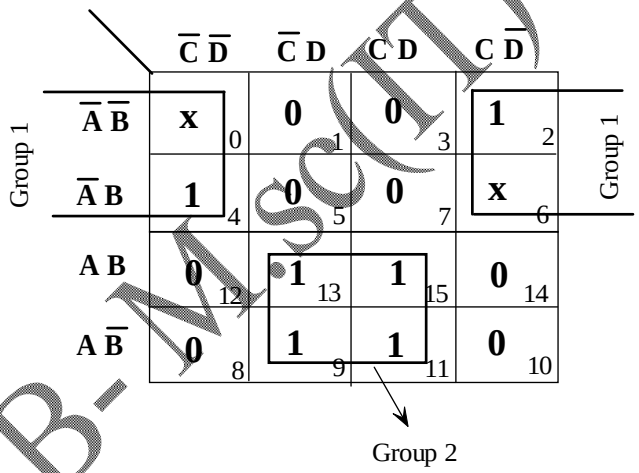


Figure.5 K-map of Function F2

From the map

Group Number	Minterms involved	Reduced to
Group I	0, 2, 4, 6	$\overline{A}\,\overline{D}$
Group II	9,11,13,15	A D

Hence F2 is reduced to

$F2 = \overline{A}\,\overline{D} + A\,D$

Which is the XNOR function, and it is implemented using the available XOR gates as

$F2 = \overline{A}\,\overline{D} + A\,D = A \oplus \overline{D}$ since $A \oplus \overline{D} = A\,\overline{\overline{D}} + \overline{A}\,\overline{D} = A\,D + \overline{A}\,\overline{D}$

and $\overline{D} = 1 \oplus D$ since $1 \oplus D = 1\,\overline{D} + \overline{1}\,D = \overline{D} + 0 = \overline{D}$

Therefore $F2 = A \oplus (1 \oplus D)$ and implemented using two numbers of XOR gates in IC 7486 as shown in Figure.6

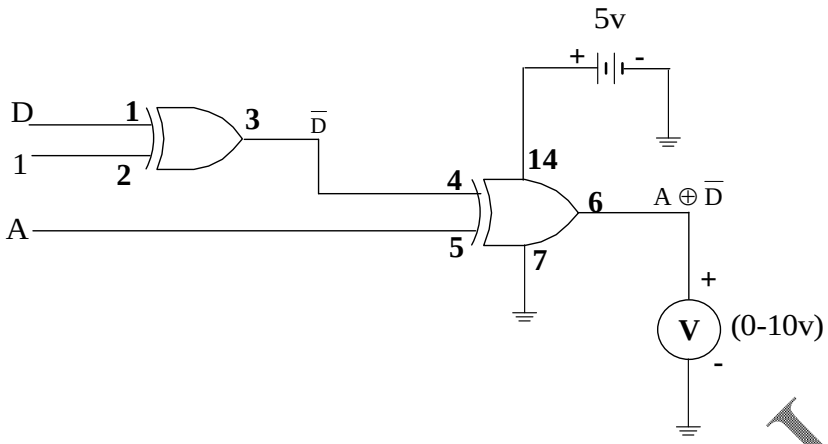


Figure.6 Implementation of Function F2 using IC 7486

TABULAR COLUMN:

1	D	$\overline{D} = 1 \oplus D$	A	$F2 = A \oplus \overline{D}$	Practical value of F2 in volts
1	0	1	0	1	
1	0	1	1	0	
1	1	0	0	0	
1	1	0	1	1	

Function F3

$$F3 = \left(\overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D} + A\,B\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,\overline{B}\,C\,\overline{D}\right) * \left(A\,\overline{C} + C\right)$$

Multiplying we get

$$F3 = A\,\overline{A}\,\overline{B}\,\overline{C}\,\overline{C}\,D + A\,\overline{A}\,B\,\overline{C}\,\overline{C}\,\overline{D} + A\,\overline{A}\,B\,\overline{C}\,\overline{C}\,D + A\,A\,B\,\overline{C}\,\overline{C}\,\overline{D} + A\,A\,B\,\overline{C}\,\overline{C}\,D$$
$$+ A\,A\,\overline{B}\,C\,\overline{C}\,D + A\,A\,\overline{B}\,C\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{C}\,D$$
$$+ A\,B\,C\,\overline{C}\,\overline{C}\,D + A\,B\,C\,\overline{C}\,\overline{C}\,D + A\,\overline{B}\,C\,C\,D + A\,\overline{B}\,C\,C\,\overline{D}$$

By Boolean laws $A\,\overline{A} = 0, C\,\overline{C} = 0, A.A = A$ and $\overline{C}\,\overline{C} = \overline{C}$

F3 is simplified as

$$F3 = 0 + 0 + 0 + A\,B\,\overline{C}\,\overline{D} + A\,B\,\overline{C}\,D + 0 + 0 + 0 + 0 + 0 + 0 + 0 + A\,\overline{B}\,C\,D + A\,\overline{B}\,C\,\overline{D}$$
$$F3 = A\,B\,\overline{C}\,\overline{D} + A\,B\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,\overline{B}\,C\,\overline{D}$$

$$F3 = \sum m(12, 13, 11, 10)$$

Thus F3 is converted to sum of minterms and mapped using the four variable map and grouping all the ones, there are two pair groups as shown in Figure.7

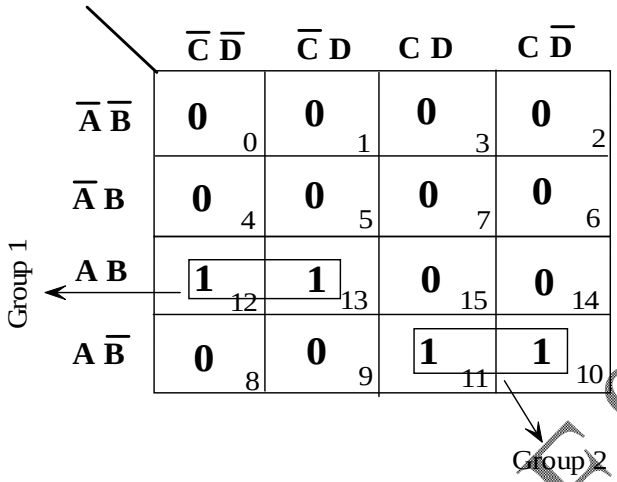


Figure.7 K-map of Function F3

From the map

Group Number	Minterms involved	Reduced to
Group I	12, 13	$A\,B\,\overline{C}$
Group II	10, 11	$A\,\overline{B}\,C$

Hence F3 is reduced to $F3 = A\,B\,\overline{C} + A\,\overline{B}\,C$

$F3 = A(B \oplus C)$

Which can be implemented using AND (one gate of IC 7408) and XOR (one gate of IC 7486) gates as shown in Figure.8

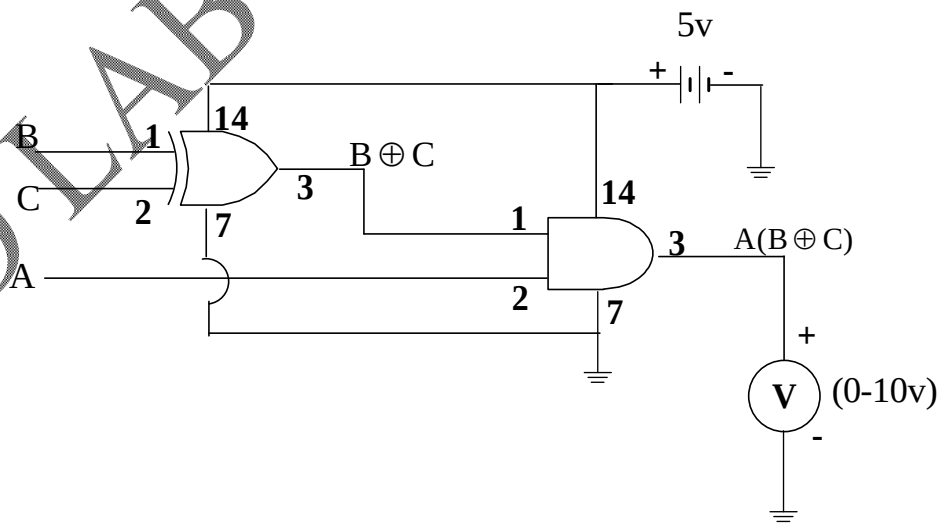


Figure.8 Implementation of Function F3 using IC 7486 and IC 7408

TABULAR COLUMN:

A	B	C	$F3 = A(B \oplus C)$	Practical Value of F3 in volts
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	0	
1	0	0	0	
1	0	1	1	
1	1	0	1	
1	1	1	0	

RESULT:

Thus logic functions are simplified and implemented using suitable logic gates.